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Vertical structure Schottky barrier diode fabrication using insulating diamond substrate

R. Kumaresan *, H. Umezawa, S. Shikata *

Diamond Research Centre, National Institute of Advanced Industrial and Science Technology, (AIST), 2-13, Central-2, 1-1-1 Umezono, Tsukuba 305-8568, Japan

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ABSTRACT

To obtain high current operation of the diamond SBDs, the device should be designed in a vertical type structure in order to minimize the device on-resistance. In this research, we have designed and developed the technology for fabrication of diamond vertical structure Schottky barrier diodes (vSBD) by utilizing Inductively Coupled Plasma etching technique. Free standing CVD grown epilayers ($p^+/p^- = 100\ \mu m/5\ \mu m$) were obtained by removing the base Ib substrate on which the epi-layers were grown, using ICP etching process. After ICP etching, ohmic contact (Ti/Pt/Au) was made at the bottom of p^+ layer, and Schottky contact (Mo) was made at top side on oxidized surface of p^- layer, to realize Diamond/Mo vSBDs and were analyzed for their electrical characteristics. The SBDs showed a reproducible ideality factor close to 1.0, and a barrier height of 1.4 eV, with a small standard deviation of 0.06 and 0.12 eV respectively. Diodes in the vertical structure exhibited R_{on} with a battery uniformity irrespective of their location on the wafer, compared the diodes in a pseudo-vertical structure. Room temperature *I–V* analysis of the fabricated vSBDs (70 µm size) exhibited a high forward current density of 2980 A/cm^2 (=0.115 A) with a low $R_{on}S$ of 8 mΩ cm^2, which could be attained due to the vertical geometry of the diodes. At the high temperature operation, still higher current density could be obtained. Satisfactory reverse blocking characteristics also could be achieved with a breakdown field of 2.7 MV/cm for small size diodes.

1. Introduction

Diamond Schottky barrier diodes can be exploited for high power applications in harsh environments [1–9]. But, the state-of-art technology for fabrication of diamond SBDs with high current operation, still finds place only on the challenging roadmap, and a well suitable technology is much anticipated [2]. Generally, semiconductor based Schottky barrier diodes are fabricated in a vertical configuration in which the current transport takes place vertically through the low resistive base substrate. In the case of diamond, in common practice, SBDs are mainly fabricated in a pseudo-vertical type configuration, using homo-epilayers grown on HPHT Ib (high pressure high temperature) diamond substrate [2–6]. This is because of the difficulty in growing low resistive diamond base substrates. There are some reports available on the fabrication of diamond SBDs in vertical structure by utilizing mesa structure with ohmic contact deposited on the etched p^+ surface, in close proximity to the mesa, or using HPHT grown diamond bulk single crystal p^+ substrates with a bottom ohmic contact layer [10–14]. But these structures have their own disadvantages, for example, in the case of mesa structure apart from the complexity of the technology, the available active layer area for Schottky contact is reduced by half, since the mesa etching is carried out around the Schottky contact. This is because the ohmic contact should have at least the same area of the Schottky metal layer, in order to draw the maximum possible current conduction from the fabricated device structure. Since the reverse electric field operation is dependent on the thickness of p^- layer, when fabricating the SBDs in a mesa structure, usually a 90 degree slope is adopted for the mesa structure, so that an uniformity of the structure in the case of all diodes could be maintained keeping in mind about achieving the similar reverse electric field operation of all the diodes. So the total area available for the fabrication of Schottky diodes on the top surface is decreased by half. Due to this reason, the current density of the device is decreased by half if fabricated in mesa structure. In the second case, the low resistive substrates grown by HPHT technique have limitation for their size and resistivity. Due to this, conventionally diamond SBDs have been fabricated in a lateral structure, containing an ohmic contact at the top of low doped p^- layer or at p^+/p^- interface via. the holes made in p^- layer. This makes the device on-resistance (R_{on}) to become high, because p^+ layer resistance [$R_{on}(p^+)$] increases with increasing distance of diodes from the ohmic contact although the p^- layer resistance [$R_{on}(p^-)$] stands to be the same, which is due to the fact that the current transport path is inclusive of both these resistances [15]. To achieve high current transport of the fabricated device, device R_{on} should be reduced. Also, achieving uniform current of fabricated diodes

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* Corresponding authors. Tel./fax: +81 29 861 2771.
E-mail addresses: drrkumaresan@yahoo.co.in (R. Kumaresan), s-shikata@aist.go.jp (S. Shikata).

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irrespective of their distance from ohmic contact, is an important factor. Both of these can be attained by fabricating the SBDs in a vertical configuration, and thus the technology for fabrication of diamond vertical structure device is highly anticipated. In this work, we have developed the fabrication technology for diamond vertical structure SBDs, utilizing Inductively Coupled Plasma (ICP) etching technique, with an intention of achieving high current transport by means of reducing the device R_{on}. Here, we reveal the details of the fabrication technology that we have developed, and the characteristics of the fabricated devices. This study throws light on the technology for achieving the high current transport SBDs based on diamond.

2. Experimental

Heavily boron doped diamond p^+ layer with a thickness of 120 μm was grown by Microwave Plasma Chemical Vapour Deposition technique on Ib (001) HPHT single crystal diamond of 300 μm thickness. After the growth of p^+ layer, p^- drift layer was grown homo-epitaxially with a thickness of 5 μm. Microwave plasma chemical vapour deposition (MPCVD) reactor (ASTEX model) was used for the epigrowth. Boron concentrations of the layers were controlled by varying B/C ratio, with the control of trimethyl borane and methane gas concentrations. The different growth conditions such as the chamber pressure, growth temperature, and microwave power, were maintained to be 25 Torr, 800 °C, 1.2 kW respectively. CH_4 was diluted with H_2 gas, and a low concentration of CH_4/H_2 with a ratio of 0.05% was used for the growth. Synthetic Ib (001) substrates with a misorientation angle of 1° was used as the base substrate.

After the epi-growth of p^+/p^- layers, the thickness of the base Ib substrate was reduced to 100 μm by scaive polishing, and then completely etched out with a removal of about 10 μm p^+ epilayer, by ICP etching technique using O_2 and CF_4 reactant gases [16,17]. The reaching of p^+ layer was realized and confirmed by the repeated etching process followed by *I–V* characterization by direct on-wafer probing method of low resistive p^+ layer. After etching process, the epi-wafer was wet chemically cleaned which consisted of Sulfuric-Peroxide Mixture (H_2SO_4:$H_2O_2 = 3{:}1$, 350 °C) soaking, followed by a hot acid treatment (a mixture of nitric and sulfuric acids), and the p^- layer surface was oxygen terminated. Towards realizing ohmic contact, Ti/Pt/Au stack layer was made at bottom side of p^+ layer by e-beam evaporation followed by annealing at 420 °C for 30 min. The sheet resistance of ohmic metal, contact layer and Schottky metal were 1×10^{-8} Ω/square, 4.7×10^{-2} Ω–4.7×10^{-4} Ω/square, and 6.5×10^{-7} Ω/square respectively. The Schottky patterns were obtained by e-beam lithography, followed by O_2 plasma ashing process to remove any residual resist, then Schottky metallization was carried out by e-beam evaporation, and the final structure was realized by lift off process. In this study the Schottky layer was made of Mo metal layer (500 Å thick, with varying sizes of 20, 30, 60, 70, 80, 100, 120, 150, 180, 200 μm diameter) on top of p^- layer to fabricate Diamond/Mo vSBDs. The process flow developed for fabrication of vSBD in this work is shown in Fig. 1. It also exhibits the schematic of vertical structure SBD (vSBD) that has been fabricated in this research. Forward conduction and reverse blocking characteristics of the fabricated vSBDs were measured using agilent-4156C source measurement unit, and beyond its limit, the high current measurement was carried out using Keithly-2612 model SMU. The *C–V* analysis was carried out using a 4284-A impedance spectroscope.

3. Results and discussion

The net acceptor concentration of the lightly doped p^- layer was estimated to be $3.7\times10^{16}\,\mathrm{cm}^{-3}$, which was deduced by the *C–V* measurement. This is a reasonable value for the adopted growth conditions. The SIMS analysis of the grown p^- layer exhibited the presence of unintentionally doped N_2 concentration to be lower than the detection limit of SIMS, in the order of below $10^{15}/\mathrm{cm}^3$. This is a good indication of a low compensation ratio in the range of below 2%, that might be highly suitable for the high current density SBDs.

Once the epi-growth was finished, the base Ib substrate was removed by ICP etching process. The maintained etching conditions are given as: $O_2 = 97$ sccm; $CF_4 = 3$ sccm; antenna power = 700 W; bias = 100 V; the etching rate achieved in this condition was 20 μm/h. To remove the Ib base substrate, first scaive polishing was carried out to remove a thickness of about 200 μm followed by the ICP etching for a period of about 6 h in steps of 2 h to avoid the overheating of the substrate as well as the ICP equipment used. The etching condition was optimized to get the after etch surface with a very minimum nano-whisker density that form during the etching process, to facilitate uniform deposition of ohmic contact. The Scanning Electron Microscopic analysis of the after etch surface exhibited a nano-whisker density in the order of $1\times10^6/\mathrm{cm}^2$, which were centred at the micro etch pits that generate during etching process, as shown in Fig. 2.

The cross sectional view of the vertical SBD as shown in Fig. 1, contained ohmic contact at the bottom side of p^+ layer and the Schottky contacts on top of p^- layer. In the present study, SBDs were fabricated in simple planar type configuration and no special mesa structure was adopted.

Fig. 3a exhibits the typical forward *I–V* characteristics (at RT) of Mo/Diamond vSBD (70 μm diameter). Forward characteristics of SBDs were governed by thermionic emission model given as:

$$J = J_s\left\{\exp\left(\frac{q(V-R_sJ)}{nk_BT}\right)-1\right\} \tag{1}$$

$$J_s = A^*T^2\exp\left(\frac{-qV_{bn}}{k_BT}\right) \tag{2}$$

where J, J_s, R_s, n, A^*, qV_{bn} are current density, saturation current density, series resistance, ideality factor, Richardson constant, and Schottky barrier height, respectively. From the forward *I–V* characteristics, SBD parameters were determined by the curve fitting procedure. The fitting parameters derived from the measured *I–V* characteristics by the fitting with thermionic emission model are given as: $n = 1.056$, $J_s = 7.5\times10^{-14}$ A/cm², and $qV_{bn} = 1.4$ eV with $A^* = 2\pi qm^*k_B^2/h^3 = 92$ A/cm² K². The ideality factor of SBDs was extracted to be close to 1.0, with a small standard deviation of 0.06, which remarks the ideal surface processing of the p^- layer surface before Schottky metal evaporation. Schottky barrier height of the diodes was estimated to be a consistent value of 1.4 eV with a standard deviation of 0.12 eV. The standard deviation is a measure of barrier homogeneity. This corresponds to a percentage error of 6 and 8.5 respectively. The lower value of the standard deviation in the present study corresponds to a more homogenous barrier height. The deviating values of the other diodes is accounted by the inhomogenous feature of the defect distribution in the epiwafer.

The fabricated SBDs showed a rectifying factor of 11 orders of magnitude. The measured R_{on} resistance of the SBDs in present vertical geometry were more uniform compared to the pvSBDs that we reported earlier [2], with the consideration of the inhomogeneous feature of defect distribution in both cases. Actually R_{on} is a function that depends on the mobility and carrier concentration of the epilayer used. Although the carrier mobility depends on the crystalline quality which should be affected by the various defects in the specimen, such as dislocation etc., these dislocations were not present accumulatively around the Schottky barrier diodes, and also the mean value of carrier concentration is constant in the wafer. Besides, there is no change in the resistance from the p^+ layer for diodes at different locations because of the vertical geometry. This causes better uniformity of R_{on} compared to the pseudo vertical structure.