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Silicon-on-Diamond — An engineered substrate for electronic applications

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Abstract

Silicon on Diamond (SOD) is a substrate engineered to address the major challenges of silicon-based ULSI technology, in particular, to provide for enhanced thermal management and charge confinement. The SOD concept is achieved by joining a thin, single crystalline Si device layer to a highly oriented diamond (HOD) layer that serves as an electrical insulator, heat spreader and supporting substrate. Therefore, SOD represents an alternative SOI concept, where the thermally insulating SiO_2 has been replaced by highly thermally conductive diamond.

Initial experiments and theoretical assessments have been aimed at demonstrating the improved thermal management properties of fabricated SOD wafers and comparing them to Si and SOI [A. Aleksov, X. Li, N. Govindaraju, J.M. Gobien, S.D. Wolter, J.T. Prater, Z. Sitar, *Silicon on Diamond: an advanced Silicon on Insulator technology*, Diamond and Related Materials, 14, 308–313 (2005).], [A. Aleksov, S.D. Wolter, J.T. Prater, Z. Sitar, *Fabrication and Thermal Evaluation of Silicon on Diamond Wafers*, Journal of Electronic Materials, 34 (2005) 1089.]. The experimental results are in good agreement with the values obtained by finite element modeling (FEM). The results show that for a 1.5 μm thick Si device layer, SOD can sustain more than 10 times higher power than SOI. This in turn will permit a more than 3-fold greater integration density of circuits fabricated on SOD as compared to SOI.

Having validated the superior thermal management properties of SOD, the second task has been to compare device operation on SOD and SOI to identify whether the Si layer degrades during the SOD fabrication process. In addition, the analysis of the interface properties between the Si device layer and diamond is important in order to better understand the operation of devices on SOD and identify their limitations. For this reason, Schottky and pn-junction diodes were fabricated on the Si device layer of SOD and SOI wafers. The first results of the electrical analyses indicated that there are no additional leakage currents in SOD devices compared to devices on SOI. In addition, CV measurements indicated no differences in the device behavior i.e. no additional charge trapping with respect to SOI in the frequency range of 1 kHz–10 MHz.

Keywords: Silicon-on-Diamond (SOD); Devices; Electronic properties; Thermal properties

1. Introduction

With every new generation of Si-based integrated circuits (ICs) one has begun to expect a doubling of the circuit complexity and clock frequency. The latter is actually a measure for the speed of the individual devices in the IC and has become a popular measure for the IC performance. In this respect The International Technology Roadmap for Semiconductors (ITRS) [http://public.itrs.net] predicts a continuation of this higher speed/complexity trend at least until 2016. However, as the predictions evolve from the present into the future it becomes clear that the main challenge in the continuing development of Si-based Ultra Large Scale of Integration (ULSI) ICs is thermal management. For 2016 ITRS predicts that chip power levels will require the extraction of 93 W/cm^2 of dissipated power, for which the technical solution is currently "not known." In addition, the reduction in device size is leading to devices with increased parasitic leakage currents, which increases power dissipation at the device level. To counter these parasitic effects, allow for lower power consumption, and increase device speed [3] Silicon-on-Insulator technology is gaining more and more momentum and is being adopted by major semiconductor chip manufacturers. In SOI, a thin (in the future ultra-thin) film of single crystalline silicon (device layer) is placed on an electrically insulating film (SiO_2), which in turn is positioned onto a thick Si handling wafer. Although attractive for reducing device parasitics, the SiO_2 layer introduces a thermally insulating barrier that presents an insurmountable obstacle for meeting the increas-

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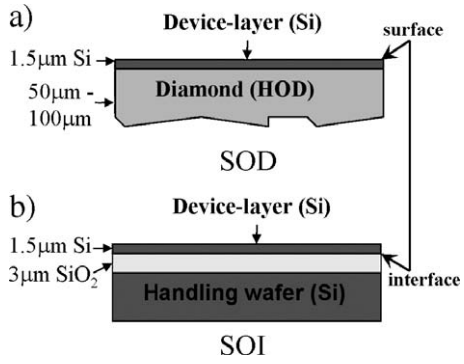

Fig. 1. Cross sections of: (a) SOD wafer, (b) SOI wafer. The connecting arrows on the right indicate that during the fabrication process [1] the SiO_2 interface side of the device layer on SOI becomes the surface side of the SOD device layer.

ingly stringent thermal management needs being posed by future electronics.

Ideally, one would like to capture the electronic characteristics of SOI within a system suitable for advanced thermal management. Silicon-on-Diamond is proposed as an alternative SOI concept where the thermally insulating SiO_2 is replaced by diamond, an electric insulator that is the best thermal conductor found in nature. In the case of SOD, the Si device layer is intimately integrated with the best heat spreader.

SOD was first suggested by Annamalai et al. in 1992 [4–6]. Later Soderbarg et al. in [7–9] demonstrated that the SOD approach was compatible with Si device fabrication technologies and could withstand the fabrication of ICs without degradation and cross-contamination. In 1998 Gu et al. [11] transferred the initial SOD concept to 4″ wafers. These experiments were primarily aimed at demonstrating the radiation hardness of SOD with respect to Si. In these studies, the diamond layer was on the order of several micrometers thick and was sandwiched between the Si device layer and the Si handling wafer, i.e. an exact copy of the SOI concept where diamond has been substituted for the SiO_2. However, the thermal management capabilities of this SOD concept will ultimately be limited by the properties of the thick Si handling wafer. In addition, the thermal conductivity of the thin diamond film will likely be limited, since the thermal conductivity of diamond films generally scales with the average grain size [10].

In the present SOD concept, a single crystalline Si device layer suitable for the fabrication of ICs is joined with a 50–100 μm thick highly oriented diamond (HOD) layer that serves as an electrical insulator, heat spreader and substrate. The reason for using HOD is supported by our studies [12] that indicate superior thermal conductivity in HOD films with respect to randomly oriented diamond. A schematic of the SOD concept is shown in Fig. 1a. The thermal management properties of our SOD wafers have been analyzed in depth with respect to SOI and Si [1,2]. This work summarizes the advantage of the thermal management properties of SOD with respect to SOI and Si. The experimental results are in good agreement with the theoretical results that were obtained by finite element modeling (FEM). In addition, we demonstrated that Si-based electronic devices can be fabricated on our SOD wafers and that they have operating parameters comparable to devices fabricated on SOI. Schottky and pn-junction diodes, were fabricated and electrically analyzed on SOD and compared to devices prepared on a reference SOI wafer. The preliminary results of electrical analyses indicated that the Si device layer has not been degraded as a result of the SOD fabrication process, and that the diodes on SOD are not plagued by additional leakage currents with respect to SOI.

2. Experimental

Details of our SOD fabrication process are given in [1]. Fig. 1a and b show cross sections of SOD and SOI wafers, respectively. The SOI wafers were procured from SOITEC and provided for a baseline comparison for SOI thermal and electronic performance, they were also used as the starting material for the SOD fabrication process. It is important to note that the device layer of the SOI wafer was transferred to the SOD substrate as described in [1]. During this layer transfer, the device layer was flipped. The surface of the device layer on SOD was originally at the interface between the Si and SiO_2 on the initial SOI, and the interface between the device layer and diamond was the surface of the device layer on SOI. This is indicated by the arrows connecting Fig. 1a and b.

Characterization of the thermal management properties of the various samples was performed by monitoring the heating behavior of resistive micro-strip heaters deposited on the sample surfaces. The heaters were fabricated using a patterned lift-off technique described in [1,2]. They consisted of an 80 nm Pt layer (the actual heater metal) and a 10–20 nm Ti layer, which served as an adhesion layer and as a diffusion barrier to suppress the formation of PtSi. Au contact leads were deposited at the heater ends and provided for a large separation between the heater and the microprobes which connected to the external circuits. This design minimized heat transport through the microprobes. Fig. 2 shows an optical micrograph of a heater and the leads. To analyze the thermal management properties of SOD with respect to SOI and Si, the temperature dependent resistivity change of the heaters at fixed power inputs was used to calculate the temperature increase experienced by the heaters deposited on the different substrates (referred to as R(T) measurements). This proved to be a very simple and effective technique since the micro strip was both the heater and the temperature sensor. Prior to the actual

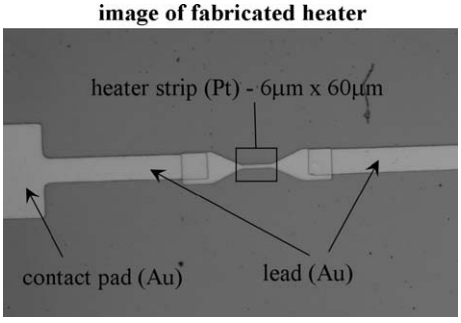

Fig. 2. Optical micrograph of a fabricated heater structure for thermal analysis on SOD.