Applied Thermal Engineering 142 (2018) 346–360

Contents lists available at ScienceDirect

Applied Thermal Engineering

journal homepage: www.elsevier.com/locate/apthermeng

Research Paper

A computational investigation of the effect of three-dimensional void morphology on the thermal resistance of solder thermal interface materials

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HIGHLIGHTS

- An innovative methodology for creating realistic 3D voids for STIM layer.
- Void morphology accounts for significant thermal resistance seen in STIM layer.
- Thermal resistance is affected by void shapes, distribution and polydispersity.
- At low void volume fraction, voids are modelled well as either spheres or cylinders.
- Thick STIM layer with high void volume fraction are best modelled using spheres.

ARTICLE INFO

Keywords:
Void morphology
Solder thermal interface materials
Thermal resistance
Microelectronics
Three-dimensional
Virtual testing

ABSTRACT

Process-induced solder voids have three-dimensional shapes and show spatially random distribution with polydisperse geometric dimensions. There exists no analytical formulation of thermal resistances which incorporates void shapes, distribution and polydispersity variables. This paper uses finite element methods to investigate the effect of realistic void morphology on the thermal resistance of solder thermal interface materials (STIMs). The study has developed two computationally efficient methods for generating voids that show the features of real voids. Cylindrical and spherical void morphologies have been studied. The study is the first attempt, in literature, of characterizing the holistic effects of such realistic three-dimensional void morphologies on the thermal resistance of STIM layers. We have shown a qualitative agreement between our results and simplistic analytical predictions. However, the influence of void shapes, distribution and polydispersity have been shown to contribute to increased thermal resistances. The findings should provide significant insight to electrical/electronics engineers, micro-electronics chips manufacturers and academic research groups working on thermodynamics design of chip scale package (CSP) devices. It is also a framework for investigating objectively, the consequence of voids on the thermo-mechanical response of solder joints.

1. Introduction

There are two main drivers that influence the current development of power devices: miniaturization and improved cooling. First, there is an increasing trend for electronic components and power devices to be miniaturized such that multiple electronic circuitry/components can be housed within a compact landscape. As well as the miniaturization trend, there exist also legislations requiring that the power devices must demonstrate improved cooling. To address these two drivers, engineers are working on innovative package designs for power devices with contemporary designs mainly based on the integrated circuits (ICs) with chip scale packaging (CSP): a very promising implementation, amongst many others [1,2].

Some of the common implementations of the CSP technology in power electronics designs include: the metal-oxide-semiconductor field-effect transistor (MOSFET) [3], ball-grid array (BGA) packages, flip-chip packages, flip-chip on flex (FCoF), integrated power electronics modules (IPEMs) [4], high-power light emitting diodes (LED) [5], etc. This paper is focussed on the flip-chip packages technology. Fig. 1 shows a schematic representation of the flip-chip CSP arrangement. The chip (silicon die) is attached to a substrate with the latter bonded onto a PCB board using the ball grid arrays interconnections. Due to the flip-chip arrangement, heat dissipation is via the backside of the chip through the heat spreader, and a possible heat sink (not shown in Fig. 1).

Effective heat management in such high power-density chip

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https://doi.org/10.1016/j.applthermaleng.2018.07.002
Received 2 April 2018; Received in revised form 26 May 2018; Accepted 1 July 2018
Available online 06 July 2018
1359-4311/

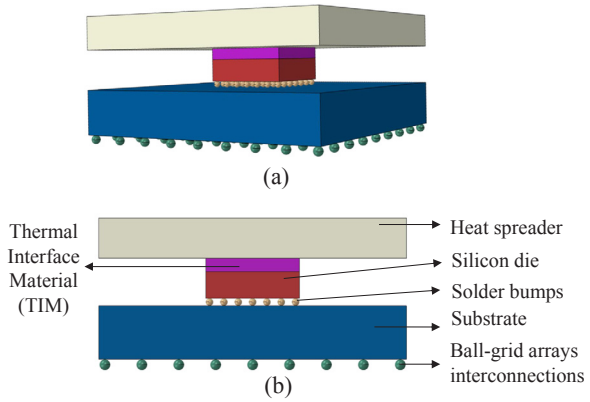

Fig. 1. A schematic representation of a typical flip-chip CSP arrangement showing (a) isometric and (b) planar views, with the different components identified on the planar view.

packages is a priority. Heat conduction between the chip (silicon die) and the heat spreader is enhanced by the introduction of a thin layer of *thermal interface material* (TIM), also called the *die-attach* [6]. The TIM suppresses interstitial air gaps [7,8] (see Fig. 2) between the mating silicon die and heat spreader components, thereby ensuring the efficient transfer of heat from the silicon die to the heat spreader.

TIMs can be either polymer-based or solder-based with the later preferred due to their better thermal performance [9]. TIMs are very important in the CSP technology and deserves careful consideration, if the desired improved cooling of the CSP package must be achieved consistently. It is important that engineers objectively quantify the thermal resistance associated with the TIM layer as this will help design reliable packages that will perform adequately over the life of the product.

Although solder-based TIMs (STIMs) are preferred to other types, a major limitation of their use in practice is their propensity for forming voids during the manufacture/reflow process of the flip-chip packages [10]. When voids form, they lead to increased thermal resistances of the TIM layer and as a result reduce the effective thermal transfer between the silicon die and the heat spreader. This raises a reliability concern for their use in design of high power-density flip-chip packages. In the last seven years, there has been sustained publications in this field and some of the commonly cited authors are given in the following Refs. [11–16].

Unfortunately, the prevalence of voids in STIMs is unavoidable due to the complex manufacturing process that solders are subjected to as well as other combination of factors, described in detail by Bušek et al. [17]. The formation of voids in solders result from outgassing during the solder reflow process, defective metallisation and poor wettability of solder [15]. The adoption of lead (Pb)-free solders have exacerbated the problem since the lead-free solders show poor solderability. Some studies have even reported more than 50% void volume fraction in some lead-free solder joints [18,19].

Some recent attempts have been made to optimize the processing history solders are subjected to, in order to limit void formation. One of the recent methods is the *vapour phase soldering* (VPS) system, also described as, *condensation soldering*. This method is a reflow soldering method considered a viable alternative to conventional and infrared soldering methods [20]. The distinctive thing about the VPS approach is that the soldering of the printed circuit board (PCB) is done within an envelop of a vapour phase of a special heat transfer fluid, such that the heat generation and transfer that completes the reflow process is through the latent heat of the condensing mass of such fluid. The main benefit for this method lie in elimination of overheat, prevention of shadowing effect (especially in large components), as well as limiting the prevalence of voiding in the solder joint [21,22]. In spite of its clear advantages, the VPS method is still fraught with such limitations as voiding (albeit limited), paste sputtering and tombstone failures [21]. Such approach and other emerging solder processing methods should serve to limit voiding in solder joints but not eliminate it completely, hence the investigation proposed here will always remain relevant to the soldering industry.

There are different classifications of voids that can be found within a solder joint for example: micro-, macro-, shrinkage, micro-via, kirkendall and pinhole voids [23]. The most common void type is the macrovoids and their diameters range from 100 μm to 300 μm, while microvoids have diameters of less than 50 μm [17]. The macrovoids are usually process-dependent voids since they are caused by the manufacturing process. The flux type and amount on void formation during the manufacturing process of solder joints was studied by Bušek et al. [17].

The impact of voids in thermo-mechanical reliability of solder joints has been studied and reported extensively. Yu et al. [24] observed that voids influence the thermal fatigue resistance of CSP solder joints. The authors observed that small voids (i.e. microvoids) have no apparent effect on fatigue life but when the voids are big, usually about 30% of the solder size, and located along the crack path, they adversely affect the fatigue resistance.

Le et al. [25] used finite element modelling approaches to investigate the effect of process-induced voids on the fatigue lifetime of lead-free solder joints subjected to thermal cycling. The authors observed that fatigue lifetime is inversely proportional to void volume fraction. Also, the location of voids affects the initiation and propagation of voids. Voids away from certain damage-prone locations did not adversely affect the integrity of the solder joints. Ladani and Dasgupta [26] used finite element modelling to investigate the effect of two-dimensional void shapes, their position, size and spacing on the durability of lead-free solder joints used in BGA packages. They concluded that voids contribute to damage initiation and evolution.

Yanus et al. [27] studied the effect of spatial representation of voids on the thermo-mechanical reliability of solder joints. The study observed that spatial positioning of the voids and their spatial distribution

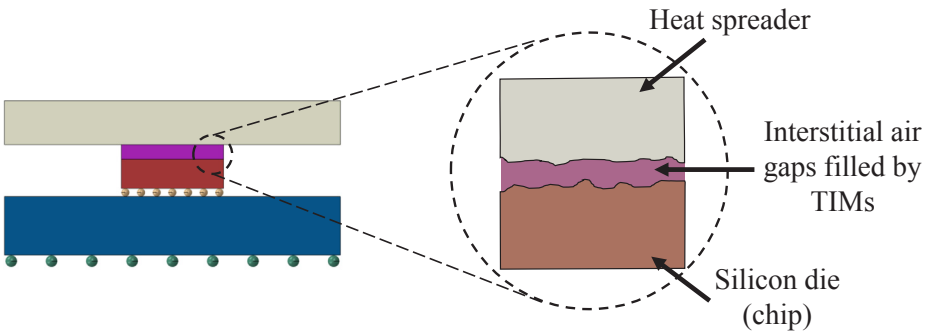

Fig. 2. Illustration of how the thermal interface materials (TIMs) are used to suppress/fill interstitial air gaps between the mating surfaces of the silicon die and the heat spreader.