



Safe-triggering-region control scheme for suppressing cross current in static transfer switch



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ARTICLE INFO

Article history:

Received 23 July 2014

Received in revised form 20 March 2015

Accepted 21 March 2015

Available online 25 May 2015

Keywords:

Thyristor-based static transfer switch

MBB

Cross current

Power supply

Voltage sags

Transfer control strategy

ABSTRACT

This paper presents a safe-triggering-region control strategy suitable for operating a static transfer switch. The suggested approach is helpful in limiting the cross current surge and enhances system's reliability. The maximum transfer time of the suggested control scheme is analyzed and found to be shorter than one cycle in all cases. The proposed approach does not require any additional components in the system. The theoretical expectations are validated by simulations and experimental results.

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1. Introduction

Modern industrial facilities comprise numerous sensitive loads, which pose increasingly higher power quality requirements [1–6]. Operation of a sensitive load can be disturbed by the common voltage sags, swells and interruptions. Recent studies [7–19] identify solid-state transfer switch (STS) as a possible cost effective solution to power quality problems. STS, see Fig. 1, is a thyristor based solid state ac switch whose task is to switch a sensitive load from a problematic feeder to an alternative feeder. STS can have a reasonably fast response and thus can reconnect an interrupted load to an alternative source within a short transfer time [7].

To control the transfer process of the STS a reliable control scheme is needed. Two common control strategies of STS are the break-before-make (BBM) [9] and the make-before-break (MBB) approaches [10]. The BBM controller transfers the load to the alternative power feeder after the primary feeder current has ceased, whereas the MBB controller initiates the transfer to the alternative line before the current has expired [10].

A clear advantage of the MBB over the BBM approach is its inherently faster transfer time. MBB method, however, is prone to errors. Under adverse circumstances, MBB controlled STS may cause an

undesirable connection between the primary and the alternative feeders. As a result, a high amplitude current surge, referred to as the cross current, may develop. The cross current may rise to a hazardous level and cause damages.

A number of studies were dedicated to the problem of STS cross current. However, the goal of eliminating the cross current surge remains elusive. Some of the difficulties arise due to the limited resolution of current sensors, the smoothing response of the current filters, and rather long current decay time [11]. To tackle the problem, [12] introduced a safe gating strategy which initialized the transfer only when phase voltage and line current in both feeders are of the same sign. However, no evaluation of the worst case transfer time was given. A control scheme, which accounts for both current and voltage conditions when employing MBB strategy, was presented in [13]. The advantage of this approach is that in case of current direction detection error, the voltage condition prevents false triggering of the thyristors. In case the current and voltage conditions are not met simultaneously, the system reverts to BBM strategy and waits for current zero crossing. Furthermore, the cross current magnitude is affected by the phase difference between the feeders' voltages [14]. Therefore, [15] attempted to eliminate the voltage differences by adding shunt capacitors [16] to the system, whereas [17,18] employed impulse Commutation Bridge to bypass the current. However, these approaches require the hardware configuration to strictly match system's parameters. And since it is difficult to reconfigure the hardware (i.e. shunt capacitors) to match

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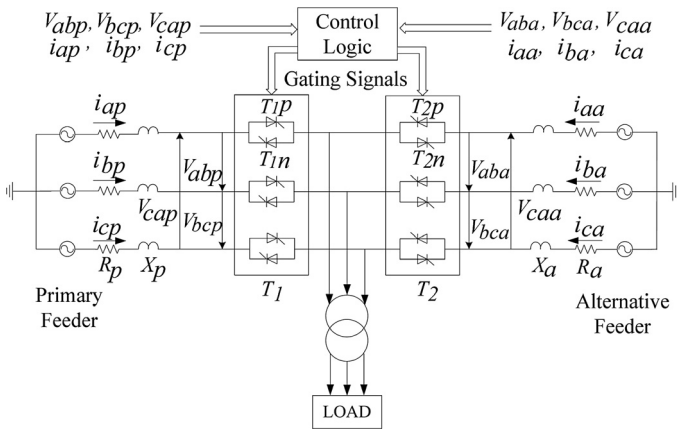


Fig. 1. IEEE STS benchmark model (STS-1).

changes in system's parameters (i.e. the phase difference between the primary and alternative feeders) application of this method seems to be difficult. In attaining the maximum transfer reliability [9], overlapping transfer of the neutral wires is introduced in [19].

This paper suggests a safe-triggering-region (STR) control strategy applicable to static-transfer-switch system. The proposed method can limit the cross current to a safe level and minimize the current stress in the power system. Analysis reveals that transfer time achieved by the proposed method is less than one cycle under all possible conditions. Theoretical predictions are supported by simulation and experimental results.

2. STS control scheme

2.1. STS model

In this study, the IEEE benchmark system STS-1 shown in Fig. 1 [10] is employed. The model in Fig. 1 has two independent sources, the primary feeder and the alternative feeder. The task of the STS is to switch a sensitive load between the two feeders.

STS in Fig. 1 is comprised of two thyristor blocks T_1 and T_2 and control logic. The control logic block of the proposed STS consists of two modules: the voltage detection module and the transfer strategy gating module. The former is responsible for detecting the voltage sags, while the task of the latter is to execute the load

transfer from the primary feeder to the alternative feeder upon detection of sag.

2.2. Quick review of BBM and MBB control schemes

As mentioned above, two common control strategies of STS are the Break-Before-Make (BBM) and Make-Before-Break (MBB). The strategy of the BBM controller is to wait for current extinction prior to issuing the transfer command. However, dependent of load, voltage sag position and type of fault, the transient process of current decay may last up to several cycles. For instance, a simulation study of a three phase short circuit fault, upstream of STS, with load power factor of 0.3 is shown in Fig. 2(a). In this case, 60 ms (3 cycles) are required for the line current to decay to zero. This simulation study exemplifies the primary disadvantage of the BBM approach, which is the long time delay needed for the BBM controller to take action. For this reason the MBB control scheme with its inherently faster transfer time is preferred [11].

The action of the MBB scheme is exemplified on the simplified one-phase model in Fig. 3. A successful MBB transfer procedure is illustrated in Fig. 3(a). It is assumed that initially the primary thyristors group T_{1p} carries the current. The transfer is initiated by firing the thyristor group T_{2p} on the alternative feeder. Thyristor T_{2p} starts conducting when forward biased. This condition arises at the instant the alternative feeder's voltage is higher than the primary feeder's voltage. As T_{2p} conducts, reverse voltage is applied to T_{1p} , which is forced to turn off, within only a few microseconds. Thus, the longest delay caused by the MBB controller is waiting for the forward-biased condition of the alternative feeder's thyristor, which is no longer than half a cycle. For these reasons, the MBB's transfer time is much shorter than that of BBM's.

2.3. Cross current phenomenon

Successful implementation of the MBB algorithm requires accurate current direction measurement and, consequently, proper thyristor triggering. However, MBB approach is known to be prone to error that may occur as a result of false thyristor triggering. For instance, if the incoming thyristor, T_{2n} , on the alternative side is incorrectly gated, the two feeders connect together as shown in Fig. 3(b). Due to low impedance between the two feeders the resulting current surge can reach unsafe level and may cause damages. This problem is referred to as the cross current problem.

Several researchers addressed the problem of the cross current [11–17]. According to [14,15], a relationship exists between the magnitude of the cross current and the phase difference between

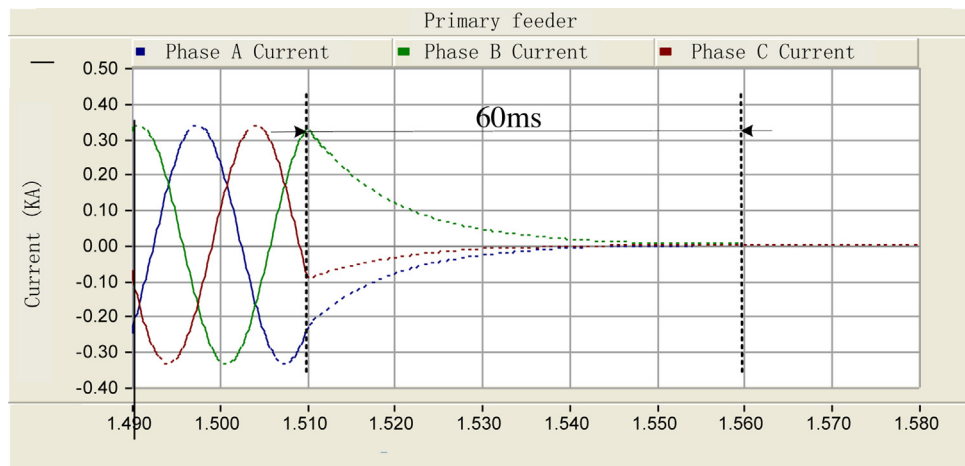


Fig. 2. Simulated waveforms of current in primary feeder during a 3-phase short-circuit fault upstream of STS (RL load with power factor of 0.3).

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