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Research Paper

Investigation of thermal characteristics and two-phase flows of a star-shape thin heat pipe

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HIGHLIGHTS

- Microchannels of a star-shape flat heat pipe were fabricated by a microfabrication process.
- Two-phase flows in the microchannels could be observed using a high-speed microscope camera.
- A VOF model was established to describe the two-phase flow in the microchannels.

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ABSTRACT

The present study develops a thin silicon-glass bonded heat pipe with microchannels fabricated on the silicon substrate. The height of the capillary wick gap was only 10 μm. Two-phase flows inside the pipe can be clearly visualized through the upper transparent glass surface. Under the observation using a high speed microscope camera, the capillary condensation and the boiling phenomena of the sealed ethanol inside the microchannels could be observed. The 3D steady VOF (volume of fluid), CFD (computational fluid dynamics) models have been established to investigate for the dynamic balance of the vapor–liquid interfaces inside the microchannels. The infrared camera measured the temperature distribution on the upper glass cover and the observed vapor–liquid interfaces inside the microchannel were applied to validate the model. The pressure drop in the condenser section could be deduced by the Bernoulli Equation using the measured vapor–liquid velocities. The deduced number (3.2 ± 0.2 Pa) was also matched the simulation result (3 Pa). As the comparison, the longitudinal thermal conductivity of the microchannel chip was about 2.2 times higher than that of the solid bonding silicon-glass plate. The concave microstructure could be useful in the WLP (wafer-level-package) stack heat dissipation module. Therefore, the microfluidic behaviors of various micrometer scale internal heat pipe structures could be investigated utilizing such a visualization platform.

1. Introduction

Since 1990, the semiconductor industry rapidly boomed following the Moor's Law. With more high density and small size dimension transistors integrated on the chip, the heat dissipation became a major target for the chip package engineers. The flat plate heat pipes (FPHP), as an efficient way for cooling and spreading the high heat flux, were widely applied in the thermal management of the integrated circuits chips [1–3]. Due to the high thermal conductivity, reliability, low weight penalty, the FPHPs are very suitable to laminate on the chip surfaces' heat dissipation interfaces. In these two-phase heat transfer devices [4], the wicks are crucial to their thermal performances. Wong et al. [5] measured the evaporation resistances of the FPHP with the sintered copper-powder. Lefèvre et al. [6] studied the FPHPs with one or two screen mesh layers capillary structures. Oro and Bazzo [7] proposed a thin micro-grooves FPHP for the Proton Exchange Membrane Fuel Cell cooling. Wang et al. [8] also presented two different FPHPs with the intersected narrow grooves and the interlaced channels respectively.

To further understanding the phenomena inside the FPHPs, the various two-phase flow models were developed. Chernysheva and

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Maydanik [9] established a three-dimension mathematical model for a flat evaporator in the loop heat pipe. Chauris et al. [10] reported a hydraulic modeling for the liquid and vapor flows inside the FPHP.

Some research groups were focused on the FPHPs' measurements. Boukhanouf et al. [11] made an analysis on the thermal performance of a FPHP using the infrared thermal imaging camera. Wong and Lin [12] studied the effects of copper surface wettability on the evaporation performance of a copper mesh wick in an operating FPHP. Lips et al. [13] deduced the capillary pressures inside the FPHPs with the longitudinal grooves. Wong and Chen [4] studied the evaporation characteristics in a groove-wicked FPHP filled with water. However, due to the complexity of the boiling phenomena inside the FPHPs, many studies still focused on the macroscopic thermal performance of the FPHPs, and did not involve the internal interaction between evaporation and condensation.

In our study, a visualization glass-silicon bonded two-phase flow star-shape microchannel chip platform was developed. The 10 μm height capillary wick gaps were fabricated by the State-of-Art microfabrication process. The transition boiling process inside the microchannels could be observed utilizing the high speed microscope camera. Hence, the effects of the micrometer scale heat pipe internal structures for the two-phase flow could be investigated.

2. Experimental section

2.1. Chip design and fabrication

To form a thin two-phase flow star-shape microchannel silicon-glass bonded visible platform, 12 "petals" were fabricated on the silicon wafer. The "petals" were served as the condenser microchannels. Each "petal" includes a 10 μm height capillary wick gap in the middle (red color in Fig. 1A), and two 150 μm height vapor pathways on the each side (brown color in Fig. 1A). The SEM image and the surface roughness profile of the etched surfaces were also presented in Fig. 1B and C respectively. During the experiments, the center area was heated as the evaporator section. Near the evaporator section, the filled liquid might be evaporated into the vapor. Then the vapor could quickly pass through the connected vapor pathways into the end area of the condenser microchannels. Due to the lower external temperature at the end area of the condenser microchannels, the vapor would be condensed in the condenser section. Finally, the condensed liquid in condenser section would be driven to the evaporator section by the capillary forces in the 10 μm height capillary wick gaps. Therefore, a typical evaporation–condensation loop could be generated.

A standard silicon microfabrication process was applied to fabricate the two-phase flow microchannels chips. The microfabrication flow chat is shown in Fig. 2. After the anodic bonding of the patterned 4″ silicon wafer (Tianjin Institute of semiconductor technology) and the 4″ Pyrex glass wafer (Suzhou Taikuni Cisco Electronics Co. Ltd.), the microchannel's filling apertures were exposed by the dicing process. The microchannel chips then were immersed into an ethanol vacuum chamber. About 70% v/v internal volume of the microchannel was filled with ethanol (Tianjin Wind Ship Chemical Reagent Technology Co., Ltd.) under a −10 psi vacuum condition. After sealing, the filled ethanol was served as the refrigerant in the microchannel chips.

2.2. Experimental setup

During the experiments, a PowerMOS transistor (Philips semiconductors, IRF830) was glued on the bottom of the microchannel chip center as the heat source. The PowerMOS transistor was driven by two DC power supplies (LODESTAR DC power supply, LP2002D; and Long Wei instruments (HK) Co., Ltd DC power supply, TPR-3010D). The high speed camera (IDT Redlake MotionXtra N-series N4, with official Motion Studio x64 software) was amounted on a standard optical microscope (Shanghai Optical Instrument Factory, XSP-8CA). The auxiliary LED light source (PI-LUMINOR100) was applied to enhance the observation illumination. The schematic plot of the experimental setup on the workbench is demonstrated in Fig. 3. An infrared video camera (FLIR A316, USA) was applied to obtain the infrared images of the microchannel chips' external surfaces.

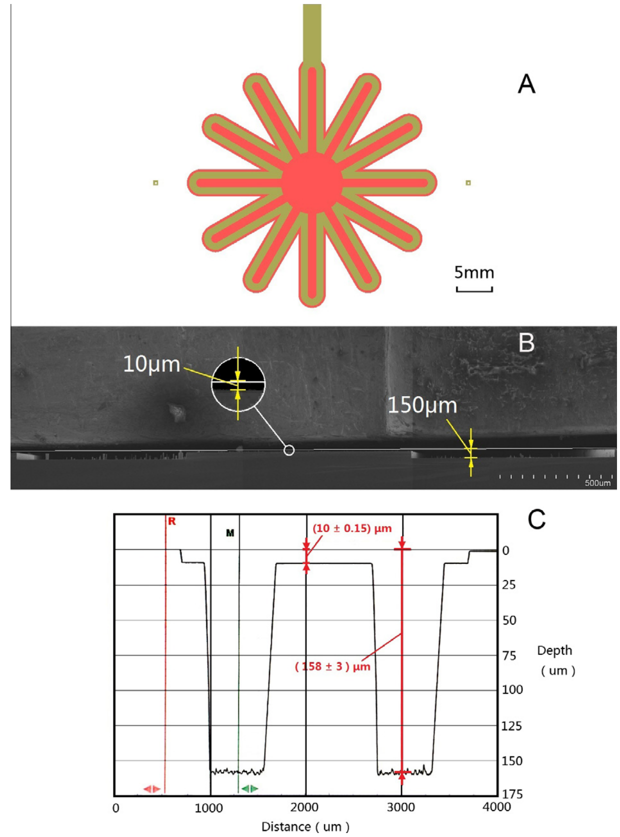

Fig. 1. (A) The mask layout of the two-phase flow microchannel. The center roundel area is the evaporator zone. The 12 "petals" are the condenser microchannels. Each channel includes a 10 μm height capillary wick gap in the middle (red color) and the 150 μm height vapor pathway on the each side (brown color). The whole microchannel chip is about 45 mm × 45 mm. (B) The SEM (Scanning Electron Microscope) picture of the microchannel cross-section. (C) The surface roughness profile of the microchannel etched area was measured by the Dektak 150 (Veeco Instruments Inc., USA). The maximum surface roughness on the 10 μm capillary wick gap was only 0.15 ± 0.03 μm, due to the wet etching process with ultrasonic. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

The CFD (computational fluid dynamics) tool (ANSYS (R14.5) FLUENT) was utilized to create the numerical simulation with the mesh tool GAMBIT (2.4.6).

3. Results and discussion

During the experiments, a commercial adjustable PowerMOS transistor (7 mm × 7 mm contact area) was affixed on the bottom of the microchannel chip center to provide a controllable heat power. Before heating, the refrigerant liquid occupied the spaces of the capillary wick gaps and part of the vapor pathways in the condensation microchannels. When the heat power was increasing, the liquid inside the vapor pathways began to move away from