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New accurate fault location algorithm for parallel transmission lines using local measurements

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ABSTRACT

This paper presents a new accurate fault location algorithm for parallel transmission lines based on the distributed parameter line model. The new method requires only voltages and currents from one end of parallel lines. Based on sequence networks and boundary conditions, equations can be derived to obtain the fault location. The new method fully considers shunt capacitance of the line, and mutual impedance and mutual admittance between the lines by using accurate model for both positive- and zero- sequence circuits, and obviates the need of iterative process to compensate for the capacitance. The method is independent of fault resistance, remote infeed and source impedances. EMTP simulation studies have been conducted to generate fault cases under various fault conditions to validate the proposed method. The results have shown that the developed algorithm can achieve highly accurate fault location estimates.

1. Introduction

Power transmission systems play an important role in delivering electric power to customers. Nowadays, the bulk transmission of electric power by means of parallel lines is widely used in the transmission systems because this structure has economic and environmental advantages over single-circuit lines. Locating a fault in a fast and accurate fashion can reduce outage time and speed up service restoration.

Many proposals for improving fault location estimation for transmission lines have been developed in the past decades. Ref. [1] shows the importance of considering the zero-sequence mutual impedance in estimating fault distance. Eriksson et al. [2] utilize phase voltages and currents from the near end of the faulted segment as input signals and consider the impact of fault resistance. In [3], an adaptive protective relaying scheme for parallel-line distance protection considering the mutual coupling effect is proposed. Izykowski et al. [4] proposed a fault location algorithm for parallel transmission lines by using the voltage and current phasors at one end, by iteratively compensating for effects of shunt capacitances. In Ref. [5], an algorithm for locating faults on transmission lines has been proposed, which copes with the effect of fault resistance. The authors in [6] present an algorithm for non-earth faults by establishing three voltage equations from one end of the faulty line to the fault point. This algorithm does not consider shunt capacitance which may cause errors for long transmission lines. The authors of [7] propose a technique of using data from two terminals of the transmission line to estimate fault location. The lumped parameter line model is adopted and the line shunt capacitance is compensated iteratively. A digital relaying technique for parallel transmission lines is presented in [8], which uses measurements from both terminals. The author in [9] proposes a digital distance-relaying technique that employs two relays instead of four relays for a parallel transmission line. Ref. [10] studies the impacts of high-resistance faults and highlights the need to include fault resistance in fault analysis. Kang and Liao [11] develop a distributed parameter line model based wide-area fault location algorithm under the availability of limited voltage measurements. Unsynchronized measurements from two terminals of the parallel line are utilized to locate the fault in [12]. The traveling wave approach is adopted in [13] for protecting parallel lines. Adaptive techniques for protection are explained in [14–18], which are intended for protective relaying applications rather than fault location.

In [19], the authors propose a method for parallel transmission line fault location using one-end data. However, shunt capacitance is neglected, which might lead to fault location errors. An iterative procedure is proposed in [4] to compensate for the effects of shunt capacitances.

This paper aims to develop an accurate fault location method for long parallel transmission lines that dispenses with iteratively compensating shunt capacitances. The equivalent PI circuit

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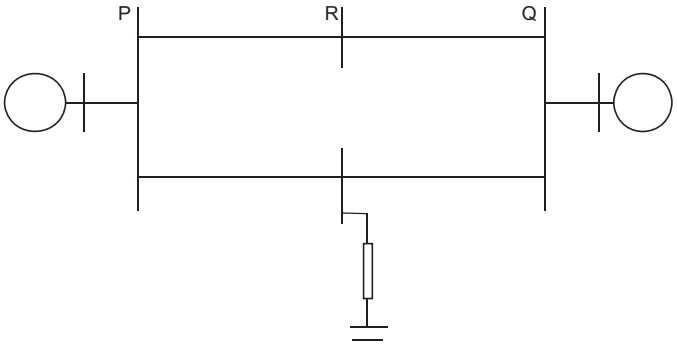

Fig. 1. Diagram of the system used to derive the proposed algorithm.

based on the distributed parameter line model, obtained in [20], is adopted. The new method, assuming the local voltages and currents are available, fully considers the mutual impedance and admittance, and shunt capacitance for accurate fault location.

The remainder of the paper is outlined as follows. The proposed fault location method is presented in Section 2, followed by the evaluation studies in Section 3. In the end, Section 4 concludes the paper.

2. Proposed fault location method

Fig. 1 depicts the system diagram used to derive the proposed fault location method, where the parallel lines are between terminals P and Q and the fault occurs at point R. First, the equivalent PI circuit models for positive-, negative-, and zero-sequence networks of the considered system are presented. Next, the derivation of the fault location algorithm is carried out. The voltages and currents of both the healthy and faulty line at terminal P during the fault are assumed to be known. The general idea of the proposed method is as follows. Based on sequence networks during the fault, sequence voltages at the fault point will be derived in terms of measured voltages and currents and the unknown fault location and fault resistance. Based on boundary conditions during the fault, the unknowns can be obtained.

2.1. The equivalent PI circuit models for different sequence networks

The positive sequence and zero sequence networks of the parallel transmission lines are depicted in Figs. 2 and 3, respectively. The parallel circuits are assumed to have the same parameters. Buses are denoted by P and Q, and R denotes the fault location. Note that in the figures, the fault is assumed to be on the second line. The notations are summarized as follows:

x parallel line indicator; $x = 1, 2$ for each of the parallel lines;

i symmetrical component index; $i = 0, 1, 2$ for zero-, positive-, and negative-sequence, respectively;

V_{ip}, V_{iq} i sequence voltage during the fault at P and Q;

V_{irx} i sequence voltage during the fault at R of line x;

I_{ipx}, I_{iqx} i sequence current during the fault at P and Q of line x, respectively;

I_{iprx}, I_{iqrx} i sequence current during the fault at R of line x flowing from P and Q, respectively;

Z_{iprx}, Z_{iqrx} i sequence equivalent series impedance of line x between PR and QR, respectively;

Y_{iprx}, Y_{iqrx} i sequence equivalent shunt admittance of line x between PR and QR, respectively;

Z_{mpr}, Z_{mqr} zero-sequence equivalent mutual impedance of the parallel lines between PR and QR, respectively;

Y_{mpr}, Y_{mqr} zero-sequence equivalent mutual admittance of the parallel lines between PR and QR, respectively;

I_{ft} i sequence fault current at R;

l total length from P to Q in km;

l_1 fault distance from P to R in km;

R_f fault resistance in ohm;

z_{isx}, y_{isx} i sequence series impedance and shunt admittance of line x per km, respectively; $i = 1$ or 2.

y, z zero-sequence self shunt admittance and self series impedance of the line per km, respectively;

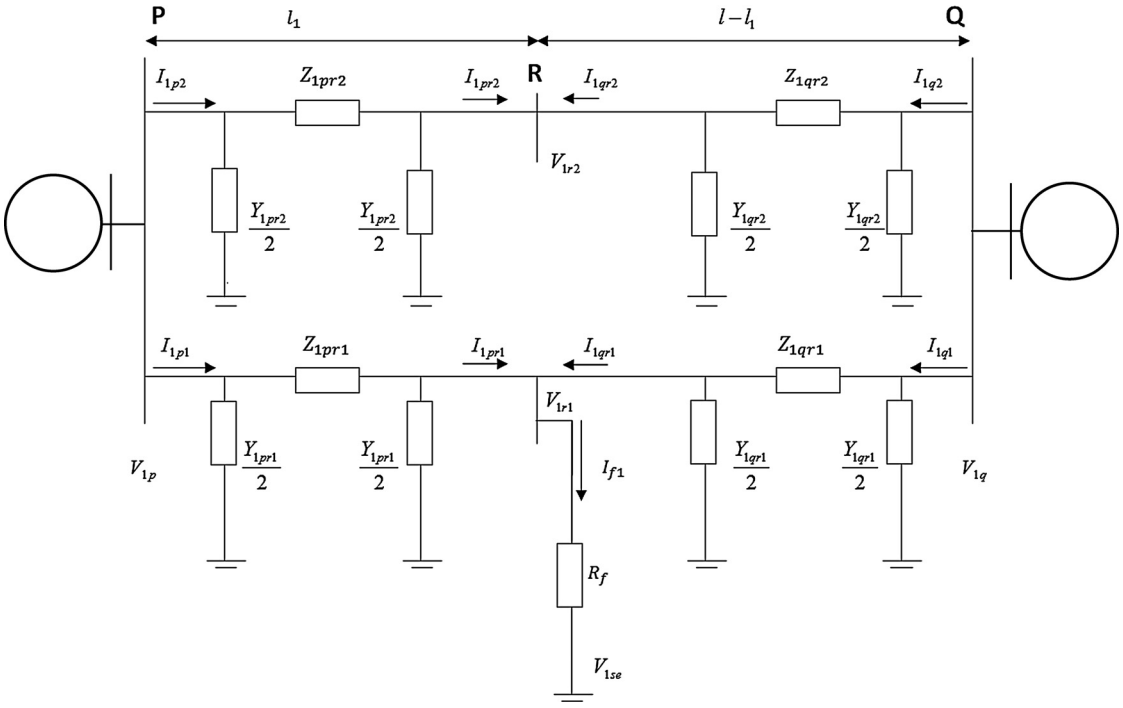

Fig. 2. Equivalent PI circuit of the positive sequence network during the fault.