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Two-stage converter with remote state pulse width modulation for transformerless photovoltaic systems

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ABSTRACT

Transformerless topologies naturally present lower cost and size and higher efficiency when compared with conventional solutions. As counterpart, these systems present high common-mode current, due to the absence of galvanic isolation, and they should have a boost stage to compensate the absence of the step-up transformer. The two-stage converter (dc–dc boost converter plus voltage source inverter) modulated by the conventional space vector modulation has the dc–dc boost stage necessary to connect the photovoltaic system to the grid, but presents high common-mode current caused by the modulation technique and the dead-time of the voltage source inverter. Therefore, a specific modulation technique that maintains the common-mode voltage of the system constant even during the inverter's dead-time is proposed, in order to reduce the circulating common-mode current. Simulation and experimental results of the two-stage converter are obtained to validate the system.

1. Introduction

The unsustainable use, in the last decades, of energy supplies based on fossil fuels triggered a growing awareness of the urgent need for renewable energy sources, such as fuel cells, solar photovoltaic (PV) and wind power [1,2]. Nowadays, the solar PV is the fastest growing renewable power technology worldwide and the majority of its installed capacity is at distribution level [3].

Due to the high generation costs and the low capacity factors of PV systems, it is essential to reduce its installation costs and increase its efficiency, aiming a competitive price for kWh and a fast payback [3]. Although massive investments have been made in the development of more efficient PV cells, modules and arrays [4], another key element of a PV system, in terms of cost and efficiency, is the interfacing stage, traditionally formed by a power converter, an output filter and a step-up transformer [5,6].

The transformer elevates the voltage level at inverter's output and provides a galvanic isolation, reducing the risk of electric shock [7]. Nevertheless, this element also increases the volume and cost of the PV system and reduces its overall efficiency by 3% [8,9]. Moreover, single-phase PV systems present a pulsating ac power on its output, requiring large dc-link capacitors that decrease the lifetime and reliability of the conversion stage [10]. For those reasons, transformerless three-phase solutions are often favored in PV applications [11].

In order to compensate the absence of the transformer, transformerless PV systems usually present a boost conversion stage. Also, due to the lack of galvanic isolation and its associated safety issue, the PV frames are always grounded [12,13]. Consequently, parasitic capacitances, which are formed between the PV array terminals and the grounded frame, should be considered. These stray capacitances, which values depend on several factors, such as the type of PV panel, the size of the frame structure and weather conditions, are estimated at 150 nF/kWp [14].

Since the parasitic capacitances create closed paths to the ground, a significant leakage current, often called common-mode current (CMC), circulates in the system, whose value depends on the common-mode voltage (CMV) generated by the high frequency pulse-width modulation (PWM) of the inverter and the resonant common-mode circuit formed by the parasitic capacitances and the output filter [11]. For safety reasons, the German standard, VDE0126-1-1, defines that PV systems should be disconnected in 0.3 s when the rms value of the CMC exceeds 300 mA [15]. Therefore, it is essential to find an efficient and low cost inverter topology and a PWM technique capable of maintaining the CMC below the 300 mA limit in transformerless three-phase PV systems.

In the last years, several solutions aiming the CMC reduction in transformerless applications have been published in literature. Initially, the authors investigated topologies and PWM techniques to reduce the CMC in ac motor drives [16,17]. For PV applications, the approach is quite different: while in ac motor drives, it is important to reduce the rms value of the CMV, in transformerless PV systems, the objective is to reduce the number of switchings and the dv/dt in the CMV. A specific design of the output filter in transformerless

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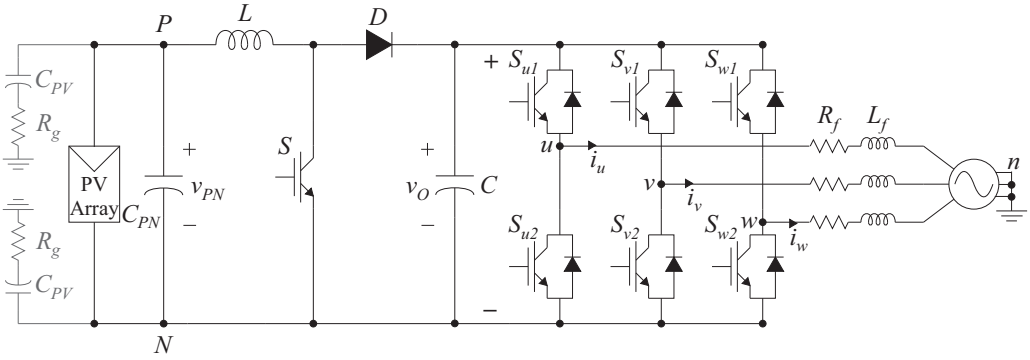

Fig. 1. TSC to reduce CMC in transformerless PV systems.

PV systems was proposed in order to shift the resonant frequency of the common-mode impedance far from the inverter switching frequency, avoiding the circulation of high CMC [18,19]. Since the values of the parasitic capacitances can span from nanofarads to microfarads, depending on weather variations, this designed resonant frequency could possibly meet again the inverter switching frequency.

Another approach was focused in modifying the inverter's topology. One simple solution is connecting the dc-link central or the negative point to the neutral point of the system [10,20]. In theory, the results are excellent, but if the impedance of the neutral cable is considered, large CMC could appear in the system. Other propositions are based on variations of the conventional voltage-source inverter (VSI) or the neutral-point-clamped (NPC) inverter, aiming to open the circulating path for the CMC when a change in the CMV occurs [21–24]. The main drawbacks of those inverters are cost and efficiency, since a large number of additional switches, diodes, capacitors and inductors are used.

In 2003, Peng proposed a family of single-stage impedance-source inverters with buck-boost capability, called *Z*-source inverters (ZSIs) [25]. The main feature of the ZSI is the cost, since it can substitute the two-stage converter (TSC), formed by a dc–dc boost converter plus VSI, with only six switches. For this reason, a few transformerless topologies based on ZSI were proposed [26–28]. Unfortunately, recent studies revealed two issues regarding ZSI-based topologies: its low efficiency, when compared with the TSC using the VSI or the NPC inverter [29]; and its stability issues, when working with low modulation index or small inductances in the impedance network [30].

Based on [29], both the conventional TSC (using the VSI) and the TSC using the NPC inverter presented similar efficiencies when applied in transformerless PV systems. Even so, the conventional TSC has, as advantage, a lower cost due to its reduced number of switches. In the field of PWM techniques for the TSC, some reduced CMV PWM techniques were analysed in [11], although none presented a rms value for the CMC below the required 300 mA limit of the VDE0126-1-1.

Therefore, in this paper, a modified PWM technique based on the remote state PWM (RSPWM) [31], is proposed for the TSC. The main feature of the proposed technique is a dead-time compensation algorithm capable of reducing not only the number of switchings in the CMV and the rms value of the CMC, but also the ripple in TSC's output currents. Simulation and experimental results for the modified RSPWM are presented, proving its feasibility. Thus, the TSC modulated by the proposed RSPWM technique becomes an efficient and low cost solution for transformerless three-phase PV systems, compliant with the VDE0126-1-1 standard.

2. Two-stage converter for PV systems

A way to guarantee a voltage boost in the converter is using a conventional dc–dc boost converter between the PV array and the VSI, as shown in Fig. 1. This topology, called TSC, combined with the RSPWM [31] guarantees the necessary voltage boost and a reduced CMC in the system. Also, this topology presents reduced number of IGBTs, diodes and passive components. The output ac voltage amplitude of the TSC is given by

$$\hat{v}_{ac} = m \cdot B \frac{v_{PN}}{2}, \tag{1}$$

where m is the modulation index of the VSI, v_{PN} is the PV array voltage and B is the boost factor of the dc–dc converter, given by

$$B = \frac{v_o}{v_{PN}} = \frac{T_{sw}}{t_{off}} = \frac{1}{1 - t_{on}/T_{sw}} = \frac{1}{1 - D}, \tag{2}$$

where t_{on} is the interval that S is closed, t_{off} is the interval that S is open and D is its duty cycle ($D = t_{on}/T_{sw}$).

2.1. Common-mode voltage in the two-stage converter

For the transformerless system in Fig. 1, a resonant circuit is created if the PV frame is grounded [32]. This resonant circuit includes PV array stray capacitances (C_{PV}), filter inductances (L_f), filter resistances (R_f) and the ground resistances (R_g).

In case of a three-phase system, the CMVs are derived between each phase, resulting in three cases: Case 1 (CMV for phases u and v $-v_{CM-uv}$), Case 2 (CMV for phases v and $w-$ v_{CM-vw}) and Case 3 (CMV for phases w and $u-$ v_{CM-wu}). For the sake of simplicity, only Case 1 is shown, since the other two cases are similar. The CMV for phases u and v can be defined as [32]:

$$v_{CM-uv} = \frac{v_{uN} + v_{vN}}{2}, \tag{3}$$

where v_{uN} and v_{vN} are the voltages between the inverter outputs and the negative terminal of the PV array.

In this paper, it is considered that the output inductances of the three phases are identical. Considering that the inverter stray capacitances are also identical, the simplified model is shown in Fig. 2(a). It is important to note this the common-mode circuit represents only the contribution of the leakage voltage v_{Nn}. Similar circuit should be considered for the leakage voltage v_{Pn}. To understand how to link the simplified two-phase circuit (Case 1) with a final model for the three-phase system, it is used the equivalent model shown in Fig. 2(b). This model can be used because the same development made for Case 1 can be applied for Cases 2 and 3. The total CMV for the three-phase inverter is calculated as [31]:

$$v_{CM} = \frac{v_{CM-uv} + v_{CM-vw} + v_{CM-wu}}{3} \tag{4}$$