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Effects of low-dimensional material channels on energy consumption of nano-devices

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ABSTRACT

It is commonly believed that the significant energy saving advantages are belonged to the logic circuits which operate at low temperature as less energy is needed for cooling them to the threshold temperature after operation. Also, nanoscale thermal management, efficient energy usage in nanoscale and especially thermal optimization are the most challenging issues, while dealing with the new generation of transistors as the miniaturizing unlimitedly the silicon channels of the transistors has resulted in an increase in the energy consumption of computers and the leakage currents. In this paper, the non-Fourier thermal attitudes of well-known two-dimensional crystalline materials of graphene, blue phosphorene, germanene, silicene and MoS_2 as the silicon channels replacements are studied by using the phonon Monte-Carlo method. We show that graphene and blue phosphorene have the least maximum temperature, representor of the reliability of the transistors, among the all five investigated nano-channels during the Monte-Carlo simulation. The established hotspots of these two materials are always cooler, not reaching the temperature threshold level, and they lose the heat much faster as the heat generation zone is switched off. The obtained results considered along with the electrical disadvantages of the graphene layer, suggests the blue phosphorene as the more thermally appropriate and optimal choice for the silicon channel replacement in new designed field effect transistors. That is to say that the limit of the energy and economic cost of the producing the advanced blue phosphorene chips meets the value of the product for the computing enterprise.

1. Introduction

Since the first silicon transistor has been launched, in the quest for higher performance, the size of these nano-devices has been incredibly decreased. Nowadays, the number of transistors on a single chip has been grown from a few thousand in the earliest integrated circuits to more than two billions [1]. In spite of the recent progress in achieving the much smaller silicon field effect transistors (FETs), the size reduction of the FETs consisting of three-dimensional (3D) semiconductors is limited by the diminution of the self-generated heat dissipation rate caused by the increase in static power and the leakage current between the source and the drain. The solution for the high energy consumption and the power devaluation have been investigated to decide the transistor contradiction of the smaller size/larger energy loss. As a consequence, FETs with channels made from two-dimensional (2D) semiconductors with almost eliminated leakage current owing to the all electrons in atomically thin channels and, accordingly uniformly influenced by the gate voltage have drawn attention [2]. Therefore, new transistor technology based on improving thermal efficiency by the usage of the channel candidates, chosen from the low-dimensional substances with odd thermal and electrical properties, such as graphene [3], germanene [4], silicene [5, 6], phosphorene allotropes [7-9] and Molybdenum disulfide (MoS_2) [10], has been activated. Each proposed low-dimensional transistor has advantages and disadvantages over the others. Therefore, the main goal of nano-electronic technology is to find the most thermally and electrically optimal nano-devices that are best suited for the substitution of the old-fashioned silicon channels and simultaneously low cost economically in cooling processes.

A decade ago, graphene which firstly attracted the attention to lower-dimensional systems, was suggested as the pioneering candidate for the silicon replacement in semiconductor device fabrication technology. Initially, the odd properties and high electrical and thermal conductivity of this appealing material made it to be announced as the perfect nominee for the transistor nanotechnology. But more studies revealed the zero bandgap of graphene which leads to the low on-off current ratios of 2 to 20. This deficiency alone, enforces researchers to behave more prudent with graphene and investigate for other matters. The current ratio, on the other hand, can be increased by shrinking the

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graphene sheet to one-dimension and manufacturing the graphene nanoribbons (GNR). Although, there are some proposals for using these nanoribbons as a silicon substitution [11], there are serious limitations for implementing the GNRs in current nanotechnology such as the reduction of the mobility from 200,000 $cm^2/V\cdot S$ to 1000 $cm^2/V\cdot S$ and difficulty in patterning the graphene in the form of GNR [12, 13]. In recent years, the FET community has shifted its interest to the sheets of advanced 2D crystalline materials which do not need to be altered to open their bandgap and have natural bandgaps of size more than 0.3 eV such that their low off-state currents and high on-state currents can be figured out. Particularly, phosphorene, silicene, germanene and mono- and few-layered transition-metal dichalcogenide systems (TMDs) such as MoS_2, have been proposed for FETs [14].

The most intriguing candidate is phosphorus, which is grouped into the graphene category. Currently, a high interest has been raised to use phosphorene as a new 2D crystalline material for electronic applications which is mainly due to its uniqueness among all 2D substances by having both an intrinsic and sizable bandgap (unlike graphene) and a high carrier mobility (unlike most transition-metal dichalcogenides). Phosphorene has different allotropes of α-, β-, γ-, δ- and ζ-phases. Although high performance FET using α-phosphorus, known as black phosphorus has been reported recently [7], the anisotropic thermal transport properties of black phosphorene may degrade the device reliability and performance since the low thermal conductivity along the armchair direction can lead the localized Joule heating in the confined system. Among the five mentioned phosphorene allotropes, it is very hopeful to use β-phase to solve the thermal management issues in the black phosphorene based FETs. Also, the interfacial thermal resistance for β-phosphorene, called as the blue phosphorene, is only a quarter to that of the graphene and this substance is more sensitive to the environmental variations than silicene [15]. In addition, a similar lattice structure and thermal conductivity to MoS_2 monolayer will make blue phosphorene a promising material to form the MOSFET channel, whose electronic properties is highly tunable by controlling the layer thickness and stacking order [8].

The other nominees for the replacement of the silicon in the transistor industry could, in fact, be silicon itself in the form of silicene, or its sister material, germanene. Silicene which is the silicon-based analogue of graphene, owing to its buckled structure, favors the existence of a bandgap of 0.21 eV and consequently the on/off ratio of 10. A parent silicon crystal, like what graphite is for graphene, does not exist in nature, but silicene is synthesized using the scalable epitaxy method. The measured mobility for both electrons and holes is about 100 $cm^2/V\cdot S$, which is quite low compared with that of graphene and blue phosphorene [5, 6] and somehow larger than the carrier mobility in the single-layer MoS_2. If we look more closely to the single layer of molybdenum disulfide, it has a large intrinsic bandgap of 1.8 eV [16] and the mobility of 0.5–3 $cm^2/V\cdot S$, which is too low for pragmatic transistor nano-devices. In practice, a 30 nm hafnium oxide, as a high-k gate dielectric on the top is used for boosting the mobility up to the value of 200 $cm^2/V\cdot S$. As a consequence, although, some works suggest these nano-materials as the promising candidates for 2D transistors, the silicene with its relative low carrier mobility and MoS_2 with its costs for making use of the full potential of it, seems not to be suitable alone for the new developed field effect transistors. On the other hand, for the formation of a germanene based field-effect transistor, a band gap opening of at least 0.3–0.4 meV is required. The band gap opens in germanene by applying an external electric field in a direction perpendicular to the germanene [17]. In similarity to the graphene, the band gap also opens by shrinking the material to nanoribbon. Accordingly, the experimental challenging existed in graphene nanoribbons fabrication also appears for germanene nanoribbons and therefore this solution for band gap opening is not the adequate one. On the other hand, the large intrinsic carrier mobility of germanene which is obtained to be a factor of 2–3 higher than the intrinsic carrier mobilities of silicene is the advantage of this material. However, germanene is not as compatible with the current silicon-based Microtechnology as silicene [18].

In all cases of energy application, more than 90% of primary energy is first converted to heat and all attempts are trying to reduce this huge amount of dissipation. This is also the important consideration while dealing with the transistors. Concerning all these new candidates of FET technology, the most important common issue is the self-heating procedure [19]. The continued miniaturization of integrated circuits and the current trend toward nanoscale electronics have led to tremendous integration levels, with hundreds of millions of transistors assembled on a chip area no larger than a few square centimeters. Circuit densities are projected to reach the giga-scale as the smallest lateral device feature sizes approach 10 nm. The bottleneck technological issue of this scaling trend is the power problem. That is to say that the chip temperatures become too large due to the self-heating and the power densities such that it prevents the reliable operation of the integrated circuits. The chip-level power densities which are currently on the order of 100 W/cm^2 will increase much as the more integration and shrinking occurs due to the International Technology Roadmap for Semiconductors (ITRS) guidelines. This high power density and self-heating makes the batteries to drain briskly in portable devices and accordingly they must be cooled to a temperature at which the transistors can operate. Consequently, as long as the cooling technology has not got up with the miniaturization many electronic devices are impractical due to the millimeter-scale hotspots on the chip, which are localized zones with higher heat per unit area and accordingly higher temperatures [20-25]. On the other hand, while chip-level hotspots are troubling circuit designers [26, 27], device designers are beginning to encounter thermal management problems at nanometer-length scales within individual transistors. Also, novel and complex device geometries tend to make heat removal more difficult and most new 2D materials being introduced in device processing have lower thermal conductivities than bulk silicon. Concerning FET, the applied voltage establishes a lateral electric field with a peak near the drain. This field accelerates the charge carriers and hence they can scatter from the other electrons, phonons, material interfaces and imperfections. The electron population gives out the energy by scattering from phonons while self-heating the lattice through the well-known Joule heating mechanism. Therefore, the Joule heating in FETs results in a local temperature rise (hot spot) where local temperatures are remarkably higher than the die average temperature. It has been obtained that among the all heat generation effects such as Joule heating, current crowding, thermoelectric, the Joule heating is evidently the dominant self-heating for low-dimensional systems [28].

In nano-electronics technology, the overall reliability is rectified by the temperature of the hottest region on the die, instead of the average die temperature. Thus, hotspots often control the required higher-level packaging and thermal management solutions including the material selections and the heat spreader design [29]. As a consequence, the thermal behavior of the nano-device and the die has a decisive role in finding the cooling requirements and controlling the impact of the environment. In other words, as the power density increases due to the growth of the temperature, the performance of the nano-device may be throttled to cause the power to decrease. Therefore, many efforts have been performed to enhance and optimize the cooling techniques for the increase of heat spreading at both the single transistor nano-device and the global die as well as the chip for minimizing the intensity and impact of the hotspots [30]. Apart from the attempts for achieving the desired methods of heat spreading, among the low-dimensional silicon replacement nominees, the one with the minimum peak temperature rise is the most optimal and appropriate choice for nano-electronics industry. This is true as the transistor cooling to keep the hottest zones of the dice under stated temperature threshold is more feasible for nano-devices with lower maximum temperatures. Indeed, the operation of the new generation transistor technology used in new modern digital devices such as laptops, tablets, and cellphones completely depends on

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