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Temperature prediction for system in package assembly during the reflow soldering process

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ABSTRACT

A system in package (SiP) is a number of integrated circuits integrated into a single module. SiP can perform various functions and are often used in small systems such as mobile phones and wearable devices. The fabrication of SiP can be challenging due to their small size and high complexity. For example, during the reflow soldering process, non-uniform temperature distribution can occur, affecting the reliability of the SiP. In this study, numerical simulation is used to investigate the thermal behavior of a SiP during the reflow process and the model is validated via experimental measurements. A forced convection reflow oven was modeled using computational fluid dynamics software where the heating of the SiP assembly was performed using a conjugate heat transfer model. A complex flow field in the reflow oven was observed from the simulation results, showing a free jet region, a stagnation flow region, a wall jet region, a recirculation region, and vortices. The simulation results agreed well with experimental data. The method developed here can accurately predict the temperature distribution in a reflow oven and allow the design of temperature profiles for the reflow process that result in minimal temperature variations across the SiP assembly.

1. Introduction

Electronic products such as cell phones, audio/video players, digital cameras, and wearable devices, require different packaging technologies. System in package (SiP) is a system integration technology that meets the demands of modern electronic devices in a feasible and cost-effective way. The SiP consists of one or more ICs with different functions, including active or passive components, assembled into a single package.

SiP assembly is produced via reflow soldering. This process is used to attach electrical components to contact pads by melting solder via a controlled heating process. The increasing complexity of integrated circuits (and hence SiP) leads to complicated thermal behavior when a circuit board passes through a reflow oven [1]. Unsuitable reflow temperature profiles can generate high thermal stresses in the package along with a variety of soldering defects [2], including bridging, solder balls, and voids, which can significant decrease the reliability of SiP assemblies.

In recent years, simulation tools for the reflow soldering process have provided useful information for the electronics manufacturing industry [1]. Prediction of the thermal distribution in the soldering process is important for the design of the outlay and control of the reflow temperature profile. In 2003, Tavárez and González modeled the thermal behavior of a solder paste pad on top of a multi-layer PCB using a multi-mode numerical heat transfer model and the finite difference method (FDM) [3]. 2-D numerical and FDM models have the limitation of not being able to model the heat transfer in all directions of a complex shape. Shen et al. [4] built a finite-element method (FEM) model to calculate the temperature distribution of a ball grid array (BGA) package for the reflow process. They assumed that the mean convection coefficient was a constant using experimental equations modeling multiple impinging jets. Inoue and Koyanagawa also used FEM to obtain the temperature field of a BGA package, and calculated the mean convection coefficient through the experimental equations of multiple impinging jets while incorporating the thermal radiation effect [5–6]. These previous methods could not model variable parameters such as the density changes in the heating gas with temperature or different fluid velocities within different heating zones in the reflow oven. Illés [7–8] experimentally obtained the distribution of the heat transfer coefficient in a reflow oven, showing that the heat transfer coefficient changes with temperature and location. In 2014, Illés [9] and Illés and Bakó [10] used CFD to simulation convection reflow ovens with a nozzle-matrix heater system. They compared two-dimensional (2-D) and

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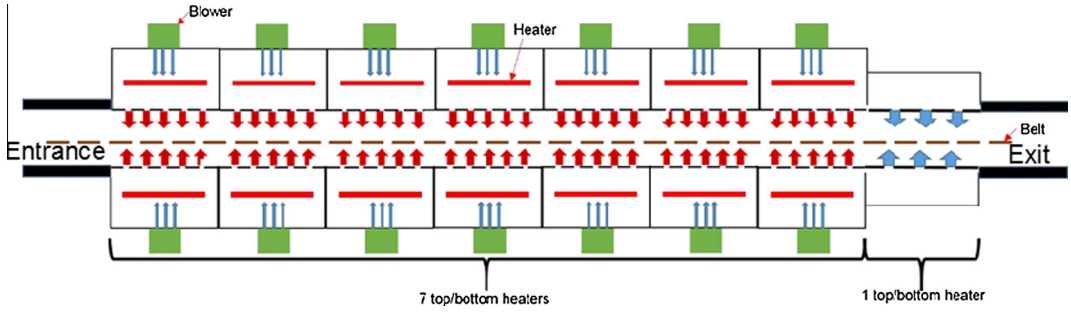

Fig. 1. Diagram of the BTU Pyramax-98N convection reflow oven.

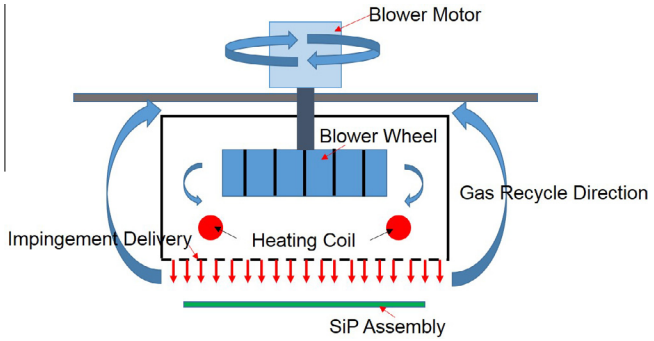

Fig. 2. Structure of the heater zone.

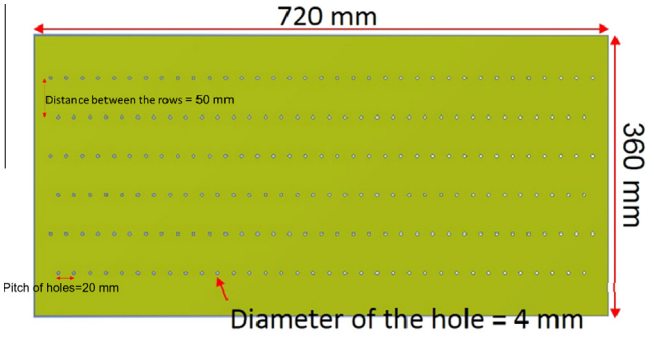

Fig. 3. Schematic of gas delivery system.

three-dimensional (3-D) simulation results of gas flow velocities in a convection reflow oven and suggested some design rules for the reflow process.

The methodology developed in this study may be used for accurate prediction of the temperature distribution in an oven as well as for designing a thermal profile for reflow soldering production with minimal temperature variation over the SiP assembly.

2. Materials and methods

2.1. Reflow oven

In this study, a BTU Pyramax-98N convection reflow oven was used with a nozzle-matrix system to form the gas streams. Reflow ovens have three major types: infrared, convection, and vapor phase. The BTU Pyramax-98N is a common convection-type reflow oven, which uses fans to force heated air toward the assemblies. A schematic diagram of the BTU Pyramax-98N convection reflow oven is shown in Fig. 1. The reflow oven consists of an entrance, seven heating zones, a cooling zone, and an exit section. The top and bottom of the heating zones are equipped with a heater. The structure of the heater zone is shown in Fig. 2. The gas (nitrogen) was heated via a heating coil and then passed over the SiP assemblies using a blower. Finally, the gas passes through the recirculation area to complete the cycle. The gas delivery system is 360 × 720 mm in size with an array of 4 mm holes (50 mm spacing between the rows and 20 mm spacing between the holes). In this study, the speed of the conveyor belt transporting the SiP assembly through the oven was 1.23 cm/s (see Fig. 3).

2.2. SiP assembly

The sample SiP assembly used in this study was made by ChipMos Technologies Inc. (Tainan, Taiwan). The SiP assembly was rectangular, with a length of 239 mm and a width of 66 mm with 72 (4 × 18) units, each of which were 12 mm × 12 mm. The thickness of the board was 0.3 mm. A photograph of the SiP assembly is shown in Fig. 4.

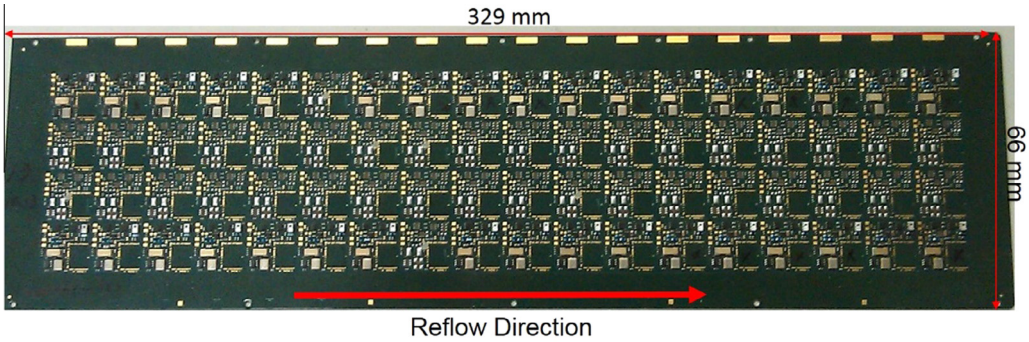

Fig. 4. SiP assembly.