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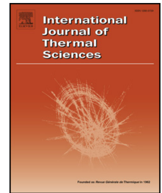
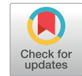


Practical analytical modeling of 3D multi-layer Printed Wired Board with buried volumetric heating sources



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ABSTRACT

Ceaseless efforts have been made by the electronic companies to increase the density of electronic boards. A new design concept consists of burying active and passive electronic components inside inner layers of a Printed Wiring Board (PWB). However this alternative leads to higher thermal stress due to heat concentration at the core of a temperature-sensitive substrate.

In order to help the electronic designers to find the optimum placement of these heating devices, a guideline based on analytical approach model is proposed. This presented work focuses on the steady-state solution of the heat equation, resolved by separation of variables and the use of Fourier's series. The domain is an anisotropic, multi-layer parallelepiped, submitted to uniform heat transfer coefficients on its upper and lower surfaces and assumed adiabatic edges. These assumptions can be employed, with confidence, to valid the predictions of chip temperatures at laboratory conditions.

To determine its ability to predict the maximum operating temperature of a set of buried chips, that practical solution is compared to its corresponding numerical model representing all the layers of realistic electronic board. Moreover the need to consider each PWB's layer is debated with the aim to faster the chip temperature evaluation. Thus a layer-selection method is investigated to find the best balance between accuracy and computation time. By using such optimised approach the computation time can be shortened by a factor of 600, compared to a detailed numerical analysis, while keeping a similar accuracy. Further, it could be a practical way to proceed to a smart simplification of the numerical model of PWB substrate for actual equipment.

1. Introduction

The endless demand for higher electronic functions drives innovation in Printed Wired Board design as well as the miniaturization of electronic components. To increase the density of conventional Surface-Mounted-Devices (SMD) on electronic boards, the burying of active chips and passive devices, into organic substrate layers, appears to be an attractive solution.

This new concept consists in the integration of very thin electronic components into laminated build-up layers, defined as “Core layers”. Then these ones are sandwiched between conventional multi-layered substrates as seen in Fig. 1.

However the integration of dissipating devices at the heart of the PWB exacerbates the need of adequate cooling. Commonly, the heat generated (Joule heating) by these buried chips is spread by conduction through the board and then removed by free-convection from its largest external surfaces, or via cooling structures regions attached on PWB. Thus, an optimum placement of the electronic components is mandatory to keep the inner temperature under the PWB in-use limit, usually 100 °C.

By consequence, electronic designers need a tool to quickly estimate the thermal constraints of their new designs. An analytical model of a multi-layered board with volumetric inner heat sources was established in that matter.

Various approaches have been developed concerning the analytical modelling of heat dissipation inside multi-layer ICs. A short overview of the relevant literature is commented below.

First, the layers can be replaced by thermal resistances in series where the heating elements are modelled by incoming heat flux at a node, as seen in Refs. [1,2] and [3]. Despite fast computation time, the spatial one-dimensional aspect of this resistance network limits the interest of this model, but new concepts are overcoming this issue [3].

Other approaches, based on Fourier's heat equation, are also available such as Fourier's series method [4–8], Laplace transform method for transient study [9] and [10], Green's function method [11] and [12] or also inverse problem technics [3] and [13]. Recent works address the

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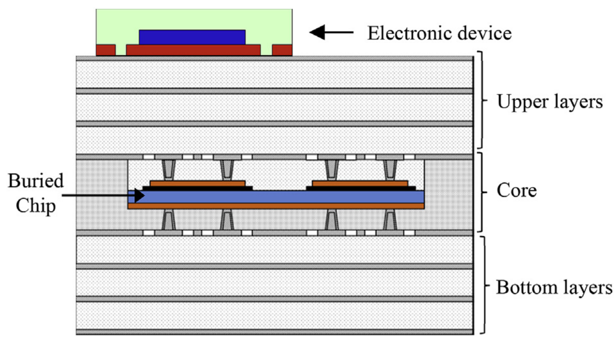

Fig. 1. Schematic cross-section of a buried chip into a Printed Wired Board.

issue of non-Fourier domain, such as the Guyer-Krumhansl type heat equation [14].

However, all these methods assume planar heat sources generally sandwiched between two layers as in Refs. [8] and [9] and also in Refs. [15–18]. A case of volumetric heat sources into a multi-layer domain is discussed by Nakayama in Ref. [19] but the developed model is dedicated to 2-D geometries having a symmetric plane.

The current study suggests, this time, considering an approach based on volumetric heat sources, which will be buried everywhere inside a set of given dielectric layers of the PWB structure. A steady-state three-dimensional solution of heat equation is resolved by separation of variables and the use of Fourier's series, as already outlined in Ref. [20].

Obviously such analytical model does not intend to replace the full detailed CFD simulation of an electronic board. Its main purpose is to provide a practical analysis tool devoted to early design phase. Moreover, its temperature predictions will also allow direct comparability to infrared radiation measurements made at laboratory condition.

The effect of localised high copper concentration areas such as vias is not handled by the PWB multi-layer stack-up but the current analytical approach can be implemented as described in Ref. [21]. Nevertheless, a realistic multiple-lumped board model is able to take into account the isolating role of the dielectric base material, an approach more relevant than unreliable "effective thermal conductivity" models based on single-cuboid board representation as demonstrated in Refs. [22] and [23].

Eventually, the developed model can be useful to provide designers means to limit excess temperatures before setting up heavy and complex CFD simulations.

2. Analytical model for embedded heating source

A steady-state analytical model of the cooling of an embedded chip within a multi-layered electronic board is developed in this following chapter.

The assumption of a coupled free convection and thermal radiation is assumed to cool the multi-layered board structure. However, multi-path heat conduction through several structure attachments placed on various locations on the PWB external surfaces can be added as well, as established in Refs. [24–26]. Indeed, in case of confinement such as consumer electronic applications (mobile phones, laptops ...), the heat conduction becomes the predominant cooling mode.

2.1. Multi-layer PWB with adiabatic edges

The spatial three-dimensional modelling of a multi-layer PWB was put in motion in Ref. [27]. In that initial work, the η layers of the PWB structure were resumed in three groups of layers as described in Fig. 1. Thus, a "core layer" was assumed, where the source is located, that is sandwiched between two external layers cooled by their external

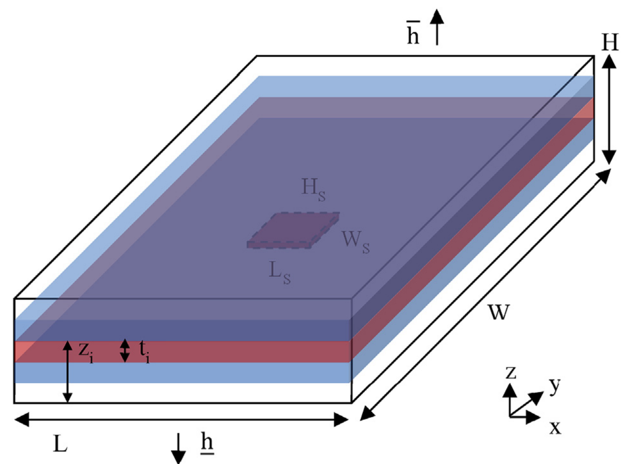

Fig. 2. Three-dimensional multi-layer PWB with volumetric embedded heat source.

surfaces in contact with the fluid.

In the current study an extension of that analysis is discussed, where the calculation of η-layers stack-up is solved. Hence, the heating chip can be allocated to any inner layers. Each layer is labelled with the index "i" as seen in Fig. 2, and is considered anisotropic. Their three axis thermal conductivity values are defined as kx_i, ky_i and kz_i.

The bottom surface of the first layer and the top surface of the upper layer are submitted to a uniform heat transfer coefficient, respectively called $\underline{h}$ and $\overline{h}$. The four lateral edges of the board are assumed adiabatic due to low PWB thickness [8,19] and consequently negligible heat losses in comparison with those of in-plane surfaces.

Thus the generalized spatial steady-state three-dimensional governing equation of any layer is:

$$kx_i\cdot\frac{\partial^2\theta_i}{\partial x^2} + ky_i\cdot\frac{\partial^2\theta_i}{\partial y^2} + kz_i\cdot\frac{\partial^2\theta_i}{\partial z^2} + \delta\cdot\dot{q}_i = 0 \tag{1}$$

Using the temperature differential form:

$$\theta_i = \theta_i(x,y,z) = T_i(x,y,z) - T_\infty \tag{2}$$

The Kronecker parameter δ is equal to 1 when a heating source is allocated to the layer.

The volumetric heat flux of the semiconductor chip is defined as:

$$\dot{q} = \frac{q}{L_S\cdot W_S\cdot H_S} \tag{3}$$

Where L_S and W_S and H_S are the dimensions of the parallelepiped heating source respectively according with x or y or z axis with centrum coordinates x_C and y_C and z_C.

The boundary conditions of the developed model are summarized below:

$$kz_1\cdot\left.\frac{\partial\theta_1}{\partial z}\right|_{z=0} = \underline{h}\cdot\theta_1 \tag{4}$$

$$kz_\eta\cdot\left.\frac{\partial\theta_\eta}{\partial z}\right|_{z=H} = -\overline{h}\cdot\theta_\eta \tag{5}$$

For PWB's edge adiabatic condition are assumed:

$$kx_i\cdot\left.\frac{\partial\theta_i}{\partial x}\right|_{x=0 \text{ or } L} = 0 \tag{6}$$

$$ky_i\cdot\left.\frac{\partial\theta_i}{\partial y}\right|_{y=0 \text{ or } W} = 0 \tag{7}$$

Where the parameters, called L, W and H, are the dimensions of the cuboid substrate according respectively with: x-axis, y-axis or z-axis.

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