Control Systems of Single-Phase Voltage Source Inverters for a UPS

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Abstract: This article presents considerations of the effectiveness of suppressing output voltage distortions of low power single-phase voltage source inverters (VSI) dedicated for UPS systems working with the nonlinear rectifier *RC* load defined in the EN 62040-3 standard. Various types of control systems were tested – PID/CDM and deadbeat instantaneous controllers designed using the author's discrete model (including the design of the output filter) of VSI and the fuzzy controller. It was shown that the additional control loop with the repetitive controller or additional input variables (currents) of the controller should be used for lowering the THD of the output voltage for the nonlinear load. The results of the experimental verification are shown.

Keywords: voltage source inverter, coefficient diagram method, repetitive control, fuzzy control, deadbeat control, nonlinear load.

1. INTRODUCTION

The output voltage quality is the basic advantage of voltage source inverters (VSI) for UPS systems. The sinusoidal PWM is typical for single- or three-phase UPS systems while space vector modulation is the standard in three-phase induction motor control systems. Single-phase inverters with output power up to 3 ÷ 4 kVA are typical for a UPS for computer systems. So the demands on them should be precisely established. The EN 62040-3 standard limits the Total Harmonic Distortion (THD) of the output voltage for the defined nonlinear load and presents the requirements for the transient response depending on the class of the system. The IEEE 519 standard specifies the demands concerning the maximum THD and the highest harmonic amplitude of the supplied voltage in the steady state. Considering the output voltage harmonics of the PWM inverter it can be easily proved that the harmonic with the highest amplitude before filtering has the frequency f_c (f_c - frequency of the modulated waveform) or $f_c \pm f_m$ (f_m - fundamental frequency of the modulating sinusoidal signal) where $f_c > 50 f_m$ is usual in UPS systems. The design of the output filter is based on the requirement to sufficiently suppress them (Rymarski 2009, 2010, 2011a) and to minimize the reactive power in the output filter components. The IEEE-519 standard does not specify the limit of the highest order of the harmonics spectrum considered. So it can be used for the design of the output filter. The EN 62040-3 standard presents demands for the low frequency harmonics (<40) at the supplied voltage. The low-order harmonics can be reduced practically only by means of the feedback loop. That is why the EN 62040-3 standard is useful for the assignment of control loop requirements. The 3-phase inverters control for a balanced load can be easily designed using the Clarke transform where a 3-phase control system is changed into two orthogonal single-phase systems. An interesting approach is presented in (Li et al. 2008) where the three-phase three-legged VSI is decoupled into two buck converters in every 60° region. The Clarke transform is very convenient as long as the balanced load is assumed. Most authors design the 3-phase balanced system and only check its behavior for an unbalanced load (e.g. Kawamura et al. 1988). The resistive-inductive *RL* load is a typical industrial load however the EN 62040 standard contains the statement that a nonlinear rectifier *RC* load with a power factor equal to 0.7 is the typical load for UPS systems for output power below 3 kVA. Most low output power UPSs are predicted to supply computer systems with AC/DC switching mode supplies with the rectifier in their input. This load is defined in the EN 62040-3 standard and the THD of the output voltage should be reduced below 8% (for the S class of the UPS). Two types of inverter control systems can be considered. The traditional control systems based on the discrete model of the inverter and the fuzzy control system based on "control rules". The presented discrete PID controller has its origin in a continuous controller; deadbeat controller is unique for discrete systems and has some parameters (the control speed) that are unreachable in continuous systems (Astrom el al. 1997) but it is more sensitive to load changes (Ben-Brahim et al. 2003). The aim of this paper is to show how the different types of the control systems influence on the output voltage quality of single-phase, 3-level voltage source inverter for a standard nonlinear load.

2. VSI OUTPUT VOLTAGE FOR THE OPEN FEEDBACK LOOP

Let us assume a low power inverter with the apparent output power S=1150 VA (V_{OUTRMS}=230 V, I_{ORMS}=5 A). According to EN 62040-3 the peak-to-peak voltage ripple on the load capacitor should not be higher than 5%. For the presented inverter the parameters of the nonlinear load (EN 62040-3) should be:

$R_S = 0.04U^2/S = 1.84\ \Omega \approx 2\ \Omega$,

V_{CO}=1.22V_{OUTRMS}=280.6 V
R_O=V_{CO}^2/(0.66S)=103.737 Ω ≈100 Ω
C_O=7.5/($f_m R_O$)=1446 μF≈1500 μF
where V_{OUTRMS} – rms value of the inverter output voltage.

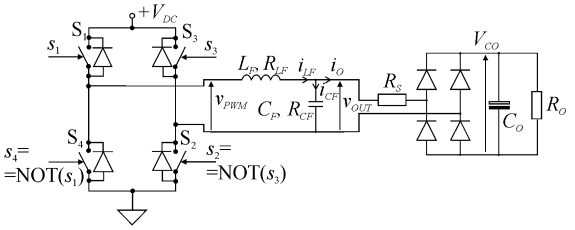

Fig. 1. A single-phase inverter with a standard (EN 62040-3) nonlinear load.

The distortions of the output voltage depend on the design of the output filter. The output filter design was presented in (Rymarski 2009, 2010, 2011a) and was based on the approach of Dahono et al. 1995. The reduction of the highest amplitude of harmonics (close to f_c frequency) below 3%, and THD below 5% (IEEE-519) was the assumption of the output filter L_FC_F product value calculation. The particular L_F and C_F values (for the known L_FC_F product value) were calculated to minimize the reactive power in the output filter components (Dahono et al. 1995). The considerations in this paper are limited only to single-phase 3-level VSI with a double edge PWM. The simplified calculation of the L_F and C_F output filter parameters is:

$$L_F = \frac{1}{f_c}\frac{V_{OUTRMS}}{I_{ORMS}},\ C_F = \frac{1}{f_c}\frac{1}{V_{OUTRMS}/I_{ORMS}} \tag{1}$$

where V_{OUTRMS} and I_{ORMS} are the rms values of the inverter output voltage and current. The calculated values in the presented example are L_F=1.8 mH (R_{LF}=0.5 Ω), C_F=0.85 μF, R_{CF}=0. The design of the output filter has a strong influence on the discrete model of the inverter and as a result on the design of the controller. Most authors that present control techniques in inverters significantly lower the value of the filter inductance and increase the value of the filter capacitance (Ben-Brahim et al. 2003) because the value of the output inverter impedance is proportional to L_F/C_F ratio. The L_F value determines how fast the output capacitor C_O can be charged when the rectifier forward bias begins. Fig. 2 shows the output voltage waveform of the inverter without the feedback loop for a nonlinear load.

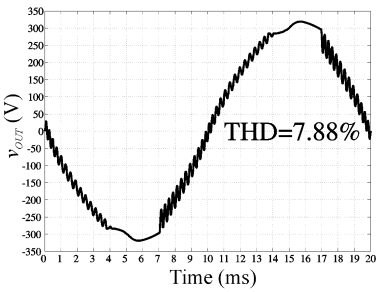

Fig. 2. Output voltage distortions for a standard nonlinear load (without the feedback loop)

When the reverse bias of the rectifier begins, the oscillating waveform that has the angular frequency ω_{RB}=1/√(L_FC_F) and the dumping factor ξ_{RB}=0.5$\omega_{RB}R_{LF}C_F$ is subtracted from the output sinusoidal voltage. When the forward bias of the rectifier begins, the oscillating waveform that has the angular frequency ω_{FB}=1/√(L_FC_O) and the dumping factor ξ_{FB}=0.5[$\omega_{FB}L_F/R_O$+ω_{FB}(R_{LF}+R_S)C_O] is subtracted from the output sinusoidal voltage. The simplified analysis of the possibility of output voltage distortion lowering is based on the calculation of the desired voltage waveform on the input of the filter to get the sinusoidal waveform on the output of the inverter with a nonlinear load (Rymarski 2010). It is not possible to force a sufficiently high step increase of the input voltage of the output filter when the forward bias of the rectifier begins in any control system for the output filter inductance L_F>$L_{F\max}$, (Rymarski 2010).

$$L_{F\max} = (R_{CO} + R_{SO})(\sqrt{2}/M - 1)/\omega_m \tag{2}$$

where ω_m=2πf_m, M is the modulation ratio in the operating point of the inverter, R_{CO} is an ESR of the load capacitor and R_{SL} is a sum of all the serial resistances of the nonlinear load. In a case where R_{CO}+R_{SO}≈R_S=2 Ω, M=0.8, f_m=50 Hz the inductance is L_{Fmax}≈5 mH. When the rectifier is forward biased the current charging the load capacitor C_O should be forced and further this current should be reduced, or for a high value of C_O this current should change its sign. Owing to the rectifier, the capacitor C_O can be discharged only through the load resistance R_O and for a high value of C_OR_O no control system can discharge the load capacitor faster (Rymarski 2010). Only systems that remember the previous fundamental cycle (e.g. the repetitive controller) or that additionally control the inductor and output currents (the multi-input deadbeat controller) can effectively reduce this type of the output voltage error. Fig. 2 presents the output voltage of the VSI with an open feedback loop and a nonlinear rectifier RC load (from Fig. 1).

3. VSI OUTPUT VOLTAGE DISTORTIONS IN INSTANTENOUS CONTROLLED SYSTEMS

The traditional design of a control system is based on the model of the plant. The discrete model of a plant (with the linearization of the control function - Kawamura et al. 1988) was presented in Rymarski (2009, 2010, 2011a). This model includes the presented design of the output filter. The transfer function of the single-phase 3-level VSI with a double edge PWM (assuming the additional one switching period delay in the modulator) is as follows:

$$V_{OUT}(z) \approx z^{-1}\frac{\left(-\sqrt{\frac{L_F}{C_F}}0.841 - 0.5R_{LF}\right) + \left(\sqrt{\frac{L_F}{C_F}}0.841 - 0.5R_{LF}\right)z^{-1})}{1 - z^{-1} + z^{-2}} I_O(z) + + 0.5z^{-2}\frac{1+z^{-1}}{1-z^{-1}+z^{-2}}V_{CTRL}(z) \tag{3}$$

In this model the load is treated as an independent current source I_O. However every real load implements a new feedback loop from the output voltage and has an influence on location of the poles of the closed loop device depending on the type and properties of the controller (e.g. time constant