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Computation of the lock-in ranges of phase-locked loops with PI filter

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Abstract In the present work the lock-in range of PLL-based circuits with proportionally-integrating filter and sinusoidal phase-detector characteristics are studied. Considered circuits have sinusoidal phase detector characteristics. Analytical approach based on the methods of phase plane analysis is applied to estimate the lock-in ranges of the circuits under consideration. Obtained analytical results are compared with simulation results.

Keywords: phase-locked loop, nonlinear analysis, PLL, Costas loop, lock-in range, pull-out frequency, hidden oscillations

1. INTRODUCTION

The lock-in concept is widely used in engineering literature (Gardner, 2005; Best, 2007). Notion of the lock-in range can be formulated in the following way (see, e.g. (Gardner, 1966)): if the difference between reference and tunable frequencies of the circuit belongs to the lock-in range, then synchronization occurs without cycle slipping (loss of cycles). In 1979 F. Gardner (Gardner, 1979) formulated the following problem: *"There is no natural way to define exactly any unique lock-in frequency."* However, *"despite its vague reality, lock-in range is a useful concept"* (Gardner, 1979).

In the present work analytical and numerical approaches for the lock-in range estimation are presented. The analytical approach is based on the integration of the phase plane trajectories and analysis of their behaviour (Tricomi, 1933; Andronov et al., 1937). The numerical approach also can be applied for the study of PLL-based circuits. However, one has to pay the special attention to results obtained by numerical simulations. Particular examples on different qualitative behaviour for two different ODE solver's step sizes can be found in (Bianchi et al., 2015; Leonov et al., 2015a).

In the present work PLL-based circuits with sinusoidal characteristics of phase detector are considered. In Section 2 model of PLL-based circuits in the signal's phase space is described. In Section 3 rigorous mathematical definitions for lock-in range are given. Methods for verifying global stability and methods of phase plane analysis are described in Subsection 3.1. Effectiveness of obtained in Subsection 3.1 lock-in range estimations is discussed in Subsections 3.2, 3.3.

2. MODEL OF PLL-BASED CIRCUITS IN THE SIGNAL'S PHASE SPACE

For the description of PLL-based circuits, a physical model in the signals space and a mathematical model in the signal's phase space are used. Models of the PLL-based circuits in the signals space are difficult for the study (Kudrewicz and Wasowicz, 2007) since the equations, which describe these models, are nonautonomous. By contrast, equations for the models in the signal's phase space are autonomous (Viterbi, 1966; Shakhgil'dyan and Lyakhovkin, 1966; Gardner, 1966), what simplifies their study.

From the numerical point of view, advantage of models in the signal's phase space is the nonexistence of high-frequency components, thus simulation in the signal's phase space allows one to consider slow varying frequency only. By contrast, the simulation of PLL-based circuits in the signals space is complicated since one has to observe simultaneously both high-frequency (fast changing of phases) and low-frequency (relatively slow changing of frequencies) oscillations. The physical models of PLL-

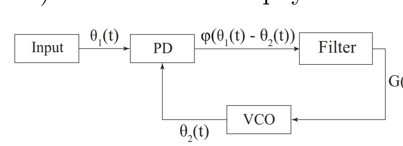

Figure 1. Model of PLL-based circuit in the signal's phase space.

based circuits can be reduced to the models in the signal's phase space (Leonov et al., 2012; Best et al., 2014, 2015;

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Kuznetsov et al., 2015a; Leonov and Kuznetsov, 2014; Leonov et al., 2015b; Kuznetsov et al., 2015b) by the averaging methods (see, e.g., (Mitropolsky and Bogolubov, 1961; Samoilenko and Petryshyn, 2004)). In order to study models of PLL-based circuits in the signal's phase space (see Fig. 1) it is necessary to compute characteristic of a phase detector – nonlinear element of PLL-based circuits for matching tunable signals. The characteristic of phase detector $K_{\text{PD}}\varphi(\theta_1(t)-\theta_2(t))$ (where K_{PD} is the PD gain coefficient) is a function with respect to the difference of phases of reference and tunable oscillators (for the model in the signals space the result of the work of phase detector $\varphi(t)$ depends on time t). Further phase difference $\theta_1(t)-\theta_2(t)$ will be denoted as $\theta_\Delta(t)$.

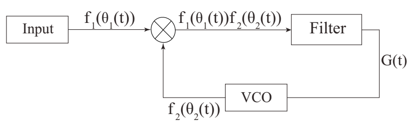

Figure 2. Model of the classical PLL in the signal space.

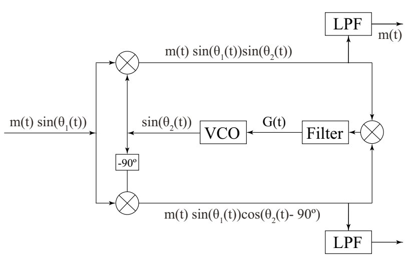

Figure 3. Realization of the BPSK Costas loop.

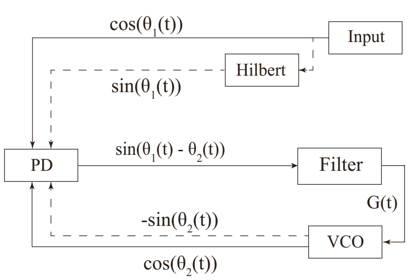

Figure 4. Two-phase PLL.

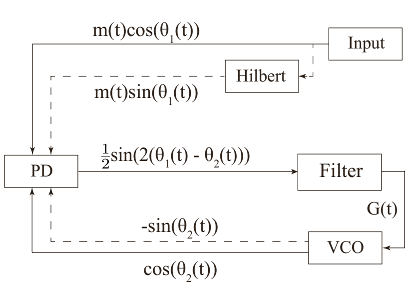

Figure 5. Two-phase Costas loop.

Let us describe a general model of PLL-based circuits in the signal's phase space (see Fig. 1). A reference oscillator and a tunable oscillator generate phases $\theta_1(t)$ and $\theta_2(t)$,

PLL circuit	
$f_1(\theta_1)=\sin(\theta_1)$ $f_2(\theta_2)=\sin(\theta_2)$	$K_{\text{PD}}=\frac{1}{2}$
$f_1(\theta_1)=\sin(\theta_1)$ $f_2(\theta_2)=\text{sgn}(\sin(\theta_2))$	$K_{\text{PD}}=\frac{2}{\pi}$
$f_1(\theta_1)=\begin{cases}\frac{2}{\pi}\theta_1+1, \theta_1\in[0;\pi],\\ 1-\frac{2}{\pi}\theta_1, \theta_1\in[\pi;2\pi]\end{cases}$ $f_2(\theta_2)=\sin(\theta_2)$	$K_{\text{PD}}=\frac{4}{\pi^2}$
Costas loop	
$f_1(\theta_1)=\cos(\theta_1)$ $f_2(\theta_2)=\sin(\theta_2)$	$K_{\text{PD}}=\frac{1}{8}$
Two-phase PLL circuit	
$f_1(\theta_1)=\cos(\theta_1)$ $f_2(\theta_2)=\cos(\theta_2)$	$K_{\text{PD}}=1$
Two-phase Costas loop	
$f_1(\theta_1)=\cos(\theta_1)$ $f_2(\theta_2)=\cos(\theta_2)$	$K_{\text{PD}}=1$

Table 1. PD characteristics and gain coefficients of the considered circuits.

respectively. The frequency of carrier signal is constant and equals ω_1:

$$\frac{d\theta_1(t)}{dt}=\omega_1. \tag{1}$$

The phases $\theta_1(t)$ and $\theta_2(t)$ enter the inputs of a phase detector. A signal of phase detector output $\varphi(\theta_\Delta(t))$ is filtered by Filter. The proportionally-integrating filter with the transfer function $W(s)=\frac{1+\tau_2 s}{\tau_1 s}$, $\tau_1>0$, $\tau_2>0$ is described by the system

$$\begin{cases}\dot{x}(t)=\varphi(\theta_\Delta(t)),\\ G(t)=\frac{\tau_2}{\tau_1}K_{\text{PD}}\varphi(\theta_\Delta(t))+\frac{1}{\tau_1}K_{\text{PD}}x(t),\end{cases} \tag{2}$$

where $x(t)$ is the filter state. In the current paper only phase detectors with sinusoidal characteristic $\varphi(\theta_\Delta)=\sin\theta_\Delta$ are considered.

The output of Filter $G(t)$ serves as a control signal for VCO:

$$\dot{\theta}_2(t)=\omega_2^{\text{free}}+K_{\text{VCO}}G(t), \tag{3}$$

where $\omega_\Delta^{\text{free}}$ is the VCO free-running frequency and $K_{\text{VCO}}>0$ is a VCO gain coefficient.

Equations (1), (3) and system (2) result in autonomous system of differential equations (here and further difference of phases $\omega_1-\omega_2^{\text{free}}$ is denoted by $\omega_\Delta^{\text{free}}$)

$$\begin{cases}\dot{x}=\sin(\theta_\Delta),\\ \dot{\theta}_\Delta=\omega_\Delta^{\text{free}}-\frac{K_0}{\tau_1}\left(x+\tau_2\sin(\theta_\Delta)\right),\end{cases} \tag{4}$$

where $K_0=K_{\text{VCO}}\cdot K_{\text{PD}}$ is the loop gain coefficient.

Analytical results on the lock-in range estimation obtained for system (4) can be applied to PLL-based circuits with sinusoidal PD characteristic: classical PLL (see Fig. 2), Costas loop (see Fig. 3), two-phase PLL (see Fig. 4), and