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Power quality improvement of radial feeders using an efficient method

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ABSTRACT

In this paper, a voltage sag compensation of Point of Common Coupling (PCC) is provided using a suitable hybrid scheme composed of a Fault Current Limiter (FCL) and a Dynamic Voltage Restorer (DVR). Current limiting task is devolved to the FCL, which has a very simple structure, along with a fast and reliable performance, low on-state losses, and low cost. The FCL not only can preserve the short-circuit level of the Distributed Generation grid (DG-grid) in a safe level, but also compensates the voltage sag for the sensitive loads connected to the PCC. The PCC feeders are classified into high-sensitive, low-sensitive, and non-sensitive feeders. In this paper, by profiting from the collaboration of the FCL and DVR in non-sensitive and high-sensitive feeders, respectively, a suitable compensation with minimum cost is suggested. The proposed compensation scheme mitigates the voltage sag and phase angle jump at the PCC. Using this strategy, a cost-effective desirable power quality for the whole loads is assured. Analytical study supported by simulation and experimental results are presented to confirm the effectiveness of the proposed hybrid technique.

1. Introduction

Keeping the Power Quality (PQ) in a pre-defined standard level is of great importance for sensitive loads in Distributed Generation grids (DG-grids). Voltage sag and momentary interruptions are among the most PQ events (about 90%), which have considerable impact on the sensitive loads [1,2]. In addition to different faults, as the main cause, voltage sag occurs due to switching of large shunt capacitor banks, transformer energizing, and starting of large motors [2–5]. Voltage sag is generally characterized by its depth and duration. The point-on-wave, where the voltage sag occurs, affects the sag parameters. Voltage sag incident has more probability in radial feeders [6]. Generally, a phase angle jump takes place in sag condition due to change of X/R ratio of the grid (R and X are resistance and reactance of power system, respectively). It is a serious problem, especially for controllers of power electronic devices utilizing phase or zero-crossing in their switching strategies [7].

With the advent of semiconductor manufacturing technologies, a large number of power electronics-based approaches have yet been proposed for solving the voltage sag problem [8]. These approaches include the use of Dynamic Voltage Restorer (DVR) [9–15], Fault Current Limiter (FCL) [16–28], Solid-State Transfer Switch (SSTS) [29], Static VAR Compensator (SVC) [30], Distribution Static Compensator (DSTATCOM) [31], Unified Power Quality Conditioner (UPQC) [32], etc. These approaches are briefly reviewed in the following:

The DVR is one of the most utilized series connected devices for compensation of the voltage sags. The DVR's function is based on the injection of a compensation voltage with suitable magnitude, phase angle, and frequency in series with the sensitive electric distribution feeder by means of an injecting transformer [9,10]. A large number of DVRs with different topologies, control schemes, and energy storage systems (ESSs) have been proposed. The main shortcoming of the DVR is that the higher active power requirement relevant to the voltage phase jump compensation significantly increases the size and cost of the DVR's DC-link capacitor. In Ref. [11], instead of increasing the size of the DVR, a new control strategy is proposed, which aims at minimizing the contribution of the DVR's active power in order to extend its compensation time. This method optimizes the gradient of the DC-link voltage by tuning the active power provided by the DVR. In Ref. [12], a new generalized voltage compensation philosophy based on the concept of series virtual equivalent impedance has been proposed. The main objective of this compensation strategy is to retrieval the difference between the sag and pre-sag conditions by injecting leading ac voltages in series with the power source. In order to reduce the control complexity of the conventional DVRs, which mostly utilize Voltage Source Inverters (VSIs), a new DVR system with cascaded multi-level direct PWM ac–ac converter is proposed in Ref. [13]. This configuration has fewer power stages and higher efficiency in comparison with the conventional DVR's topologies. Furthermore, the need to bulky DC-link capacitors is eliminated. In Ref. [14], a new multilevel cascaded-type

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Nomenclature

$\hat{V}_{PCC}()$	Voltage phasor of the PCC
$V_{PCC}()$	Voltage magnitude of the PCC
$\varphi_{PCC}()$	Phase angle of the PCC voltage
$\hat{Z}_e()$	Equivalent impedance of the feeders
X_e	Equivalent reactance of the feeders
R_e	Equivalent resistance of the feeders
(N)	Denotes the parameters in normal condition
(F)	Denotes the parameters in fault condition
(FCL)	Denotes the parameters in fault condition with FCL
$\hat{Z}_t$	Phasor of the distribution transformer impedance
X_t	Reactance of the distribution transformer winding
R_t	Resistance of the distribution transformer winding
$\hat{Z}_s$	Phasor of the source impedance
X_s	Reactance of the power source
R_s	Resistance of the power source
X	System equivalent reactance
R	System equivalent resistance
$\hat{V}_s$	Phasor of the source voltage
$\hat{Z}_{1,2,3}$	Phasor of the load impedance
$Z_{L1,2,3}$	Phasor of the feeder impedance
$\hat{Z}_{FCL}$	Phasor of the FCL impedance
$\hat{Z}_f$	Phasor of the fault impedance
L_s	Source inductance
φ_{jump}	Phase angle jump
v_m	Amplitude of the source voltage
C_r	Series capacitance of the FCL
L_{sr}	Series resonance inductance of the FCL
L_{pr}	Equivalent leakage inductance of T_1 seen by C_r in FCL
R_{pr}	Equivalent resistance of T_1 windings seen by C_r in FCL
$\vec{V}_{s,pre}$	Source voltage vector during pre-sag stage
$\vec{V}_{s,sag}$	Source voltage vector during sag conditions
$\vec{V}_{inject}$	Vector of DVR injected voltage
$V_{grid,LL}$	Rated line-to-line voltage of grid
$V_{sag,max}$	Maximum depth of voltage sag
$V_{inject,pu}$	Maximum series injection voltage in p.u.
I_{Load}	Load current
ϕ	Power angle of the load
θ	Rotating phase angle
k	Time (sample) index
f	Power system frequency
f_s	Sampling frequency
ω	Power angular frequency
ψ	Gaussian white noise with zero mean and covariance Q
ν	Random term with zero mean and covariance R
x	System state
A_{Trans}	Rated capacity of DVR transformer
$C_{DC\text{-}link}$	Inverter's DC-link capacitance
PQ	Power Quality
DG	Distributed Generation
DVR	Dynamic Voltage Restorer
FCL	Fault Current Limiter
SSTS	Solid-State Transfer Switch
UPS	Uninterruptable Power Supply
UPQC	Unified Power Quality Conditioner
SVC	Static VAR Compensator
DSTATCOM	Distribution Static Compensator
TCR	Thyristor-Controlled Reactor
TSC	Thyristor-Switched Capacitor
PCC	Point of Common Coupling
PLL	Phase Locked Loop
KF	Kalman Filter
SVPWM	Space Vector Pulse Width Modulation
VSI	Voltage Source Inverter
MOV	Metal Oxide Varistor
IGBT	Insulated Gate Bipolar Transistor
ESS	Energy Storage System

DVR structure with fault current limiting ability has been proposed. The DVR limits the fault current by activating a set of anti-parallel thyristors during the fault conditions. Similar to the structure proposed in Ref. [13], this method lowers the power rating and cost of the components while it offers an additional function of fault current limitation. Although the DVR is the most common series-compensator option, in networks with high short-circuit capacity, a bulky, high rated, and expensive DVR should be installed.

Another series-connected alternative for compensation of the voltage sags is the FCL, which can effectively mitigate the amplitude and phase angle jump of the voltage sag [16]. In fault condition, the voltage sag is proportional to the magnitude of short-circuit current. If an FCL is utilized at the beginning of most exposed radial feeders, the voltage sag would be effectively compensated at the Point of Common Coupling (PCC) [17]. Furthermore, the short-circuit level of the DG-grid is preserved in a suitable level. Subsequent to connection of a DG unit to the DG-grid, the short-circuit level increases. In such condition, the short-circuit withstanding capability of the components in the DG-grid may be lower than the increased short-circuit capacity of the network [18–21]. Several FCL structures have been proposed to reduce the transient fault currents [22]. Although superconducting FCLs have suitable characteristics, but they have many practical restrictions such as complex cooling system and high investment cost [23,24]. Available varistors can be utilized for the fault current limitation process, though they usually require a long time to be cooled down. Consequently, they cannot be used successively within several seconds [25,26]. In resonant type FCL, an inductance or parallel resonance circuit is inserted in the load current path to limit the fault current [27,28]. This approach can be implemented using varistors and/or solid-state switches [27]. Solid-state FCL as an efficient alternative can alleviate the transient current by inserting a limiting reactance, an energy absorbing element (such as resistor or varistor), or parallel resonant circuit in the load path [28].

The SSTS was initially proposed for mitigation of large fault currents. However, it is found that it can also be used for compensation of the voltage sags by selecting appropriate circuit configuration [29]. Unlike DVR that is mostly installed on the feeders supplying the sensitive loads, the SSTS should be installed on every potentially faulty line. Therefore, the overall cost of the implementation would be high.

The SVC and DSTATCOM are two shunt-connected devices, which have been used for voltage support of critical loads [30]. The SVC is composed of a thyristor-controlled reactor (TCR) and a thyristor-switched capacitor (TSC), which is often installed at the PCC bus to provide fast voltage support. The main defect of this approach is that fast response of the SVC very often leads to secondary unstable voltage oscillations [30]. The DSTATCOM is mainly composed of a modular voltage source converter and a three-phase transformer. The converter comprises Insulated Gate Bipolar Transistors (IGBTs) that are controlled using the pulse width modulation (PWM) technique. Although DSTATCOM effectively deals with the voltage transient contingencies, it does not provide active power support [31].

The UPQC has also been used to resolve the problems relevant to the voltage sags [32]. It is considered as a hybrid-connected device for PQ improvement as it is an integration of series and shunt voltage source converters. The UPQC provides both active and reactive power support. The response time of the UPQC for reactive power compensation is also very well. However, the UPQC requires a huge DC-link capacitor.

According to the above discussions, one can conclude that the foregoing voltage sag compensation methods have some inherent