Electric Power Systems Research 162 (2018) 150–160

Contents lists available at ScienceDirect

Electric Power Systems Research

journal homepage: www.elsevier.com/locate/epsr

Input-current/output-voltage ripple mitigation in the double dual boost converter

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ARTICLE INFO

Keywords:
DC–DC power converters
Power conversion
Pulse width modulation converters
Current ripple cancellation
Fuel cells

ABSTRACT

In this paper a novel switching ripple mitigation technique is developed and applied to the double dual boost converter (DDBC). Under the proposed scheme, an unconstrained selection of the voltage-gain-range at which the input-current ripple is mitigated is enabled. Furthermore, as an emerging advantage of this new strategy, we demonstrate that the elimination of the output-voltage ripple can be also achieved. The simultaneous input-current- and output-voltage ripple mitigation under a fixed but otherwise arbitrary selection of the converter's input-to-output voltage gain is the main contribution of this work, which is in sharp contrast with current switching techniques that are exclusively focused on input-current ripple cancellation at constrained duty cycles. Theoretical and experimental evidence is presented to validate the proposed scheme.

1. Introduction

Photovoltaic PV panels, fuel cells, as well as other renewable energy sources have attracted attention in the last years as a compelling alternative to fossil fuels. These systems bring important technical and theoretical challenges, e.g. the need of voltage regulation under wide load variation (load-dependent voltage) and under unpredictable environmental situations; and the requirement of high-voltage gains due to their considerably low output-voltages with respect to those induced by conventional generation plants. For instance, in a fuel cell (FC) stack, the voltage per cell is around 0.6 V nominal (cf. [1]); consequently, for high voltage DC bus requirements, a high voltage gain converter is required. Moreover, it has been observed that the use of traditional switching power converters can be detrimental for the lifetime and performance of renewable energy sources, such as fuel cell stacks, and PV panels due to the presence of significant current ripples [1–3]. For instance, the FC current ripple must be lower than 5% of its rated value, to ensure a minor impact in the device conditions (cf. [1]). In order to overcome this situation, new topologies have been designed to mitigate current ripples.

These topologies offer the additional features such as high input-to-output voltage gains. For example, quadratic boost converters (see e.g. [4–7]); however, a common disadvantage of these topologies is the high voltage stress across their capacitors and/or transistors. Other high-gain topologies based on multilevel stages have been also proposed, see e.g. [8–12]; however, though these modular configurations considerably reduce the voltage stress across components, their dynamical representation requires a high number of variables and differential equations, which brings a non trivial problem in the case of analysis and synthesis of controllers [13–15]. High-gain inductor-based topologies, such as switched inductors [16–20] and coupled inductors [21–24] are also used; unfortunately, since inductors are bulky components, their size/weight and cost might potentially become an issue. Another solution involves switched-capacitor topologies [25–27], which overcome some of the aforementioned issues, featuring small size/weight and high power density [14]; however, it is not possible to regulate the output of these converters without relinquishing at their efficiency, i.e. the converter losses are inevitably the control mechanism [28].

Other high-voltage gain topologies that also exhibit input-current ripple mitigation include [3,29–31]. There exist other remarkable solutions to decrease the input-current ripple, see for example the passive filter based on tailored coupled inductors proposed in [32], and the *double dual boost converter* (DDBC), which was initially proposed to be implemented in FC generation systems [29,33]. In the case of the DDBC, it comprises additional important advantages, e.g. in terms of costs its structure permits individual module design such as modules involving single inductors with standard low-cost commercial nominal value components.

In general it has been shown that the DDBC can achieve input-current ripple cancellation and an overall satisfactory performance in

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https://doi.org/10.1016/j.epsr.2018.05.013
Received 26 October 2016; Received in revised form 20 February 2018; Accepted 8 May 2018

experimental implementations, see e.g. [29,34]. Dynamic analysis of this topology has been also reported in [33], where its modeling and control is studied. In addition to the already reported advantages of the DDBC, in this paper we proposed an original switching ripple mitigation technique for this topology, encompassing a component-wise design and a PWM switching scheme. The new emerging advantages, due to our approach, include an arbitrary selection of the converter nominal gain associated to the complete input-current ripple cancellation. This is in sharp contrast with current approaches for which the voltage gain had to be constrained to a particular case of duty cycle. Consequently, in our proposed scheme an input-current ripple cancellation is achieved at any desired input-to-output voltage gain.

Furthermore, we show that the DDBC can simultaneously cancel out the output voltage ripple. This is achieved by a combination of a new PWM scheme and a special method to select passive components. The simultaneous cancellation of current/voltage ripple characteristic is a new emerging advantage that has not been yet available in standard interleaved converters nor in the literature. As in the current ripple case, the voltage ripple cancellation permits the use of small output capacitances for a given ripple specification. It is also possible to determine the voltage ripple in a full operation range to ensure that it is always equal or below a desired specification. The underlying analysis to calculate the input current ripple and output voltage ripple operation range is provided and a design procedure that is validated with experimental results is discussed.

2. Traditional operation of the double dual boost converter

In this section the main characteristics and waveforms of the traditional DDBC are shown. Fig. 1 illustrates a basic DDBC configuration with only two unidirectional switching stages [29,33]. The sub-circuit constituted by L_1, C_1, S_1 and $\overline{S}_1$, is defined the *upper switching stage*, while the *lower switching stage* is that containing L_2, C_2, S_2 and $\overline{S}_2$. In the circuit in Fig. 1, diodes are labeled as $\overline{S}_x$ (inverted S_x), and can be substituted by a transistor with a complementary duty cycle, if bidirectional power flow and/or synchronous rectification are required. For ease of exposition the converter is assumed to operate in continuous conduction mode. Then the upper diode is closed when the upper transistor is open and vice versa; the same consideration applies for the lower switching stage. Fig. 1 also shows the PWM scheme as well as relevant waveforms when operating with a duty cycle $D = 0.7$. The PWM is generated by two triangular carriers (Carr1 and Carr2) shifted 180°. Both inductors have the same inductance and the same duty cycle is used for both switching stages.

As it can be observed in Fig. 1, the input-current is equal to the sum of the current through both inductors minus the output-current. The input-current ripple is smaller to those through the inductors, e.g. in the illustrated case, the input current ripple is approximately 60% of the current ripple through each inductor.

Fig. 2 depicts the ratio of the input-current ripple over the ripple through each inductor, showing comparison with the traditional interleaved boost converter, when $D = 0.5$. It can be noticed that the converter achieves a perfect input current ripple cancellation. All works reported in the literature about the double dual boost converter operate with this PWM strategy, which is completely analogous to that of the classical interleaved boost converter, and in which the switching mitigation duty cycle cannot be arbitrarily selected. This issue demonstrates the advantage of our approach, for which the designer can select the duty cycle at which the input-current ripple is zero, which permits to operate the converter at the best operating range required for a given application.

3. Steady state analysis

In this section the steady state analysis of the DDBC is revisited, in this case by allowing the use of different duty cycles for the upper and

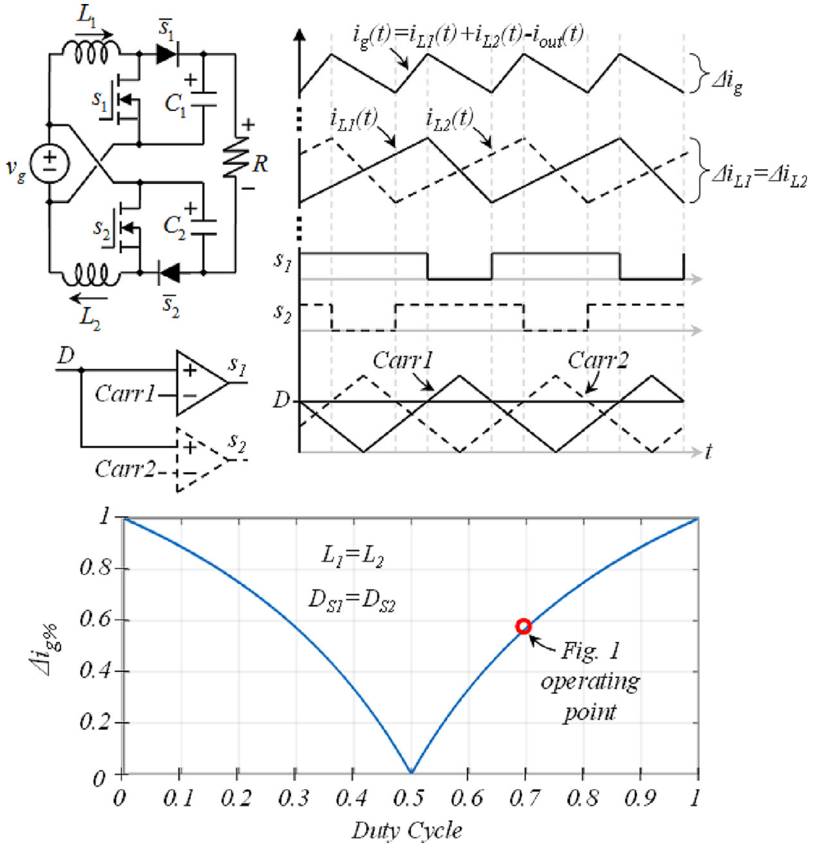

Fig. 1. Simple double dual boost converter, schematic, PWM and important waveforms when $D = 0.7$.