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A robust phase-locked loop against fundamental frequency deviations and harmonic distortions

Luiz H.S. Silva[a], Alfeu J. Sguarezi Filho[b], Darlan A. Fernandes[c], Fabiano F. Costa[a,d,*], Antonio J. Marques Cardoso[d]

[a] Department of Electrical Engineering, Universidade Federal da Bahia, Brazil
[b] Centre of Engineering, Modelling and Social Applied Sciences, Universidade Federal do ABC, Brazil
[c] Department of Electrical Engineering, Universidade Federal da Paraiba, Brazil
[d] CISE – Electromechatronic Systems Research Centre, Universidade da Beira Interior, Portugal

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ABSTRACT

This paper proposes a frequency-adaptable method for computing the phase associated with the positive sequence components from the measured grid voltages. It relies on a simple procedure in which the positive sequence is separated from the negative one through a suitable decomposition of the synchronous voltage vector onto the stationary $\alpha\beta$ frame. The procedure performance is enhanced by means of an one-cycle Fourier filter. The positive sequence voltages are then handled by a synchronous-reference frame phase-locked loop (SRF-PLL) algorithm. The structure composed of the positive-sequence estimator and the SRF-PLL is called a one cycle Fourier PLL (OCF-PLL). The OCF-PLL is robust against voltage harmonic distortions due to the OCF frequency-response characteristic. The frequency adaptability is obtained through the series connection of two OCF-PLL blocks. In the first block the fundamental frequency is computed by the SRF-PLL. This frequency is supplied to the second OCF-PLL block which computes the positive phase of the original measured voltages. Also, in this paper, the frequency adaptability is mathematically demonstrated. The method is initially evaluated by means of simulated voltages. Then, an experimental setup has been designed, in which the proposed method has been implemented in a digital signal processor (DSP) and tested on voltages produced by a programmable power supply able to emulate distorted and unbalanced voltages. The results prove the technique efficacy.

1. Introduction

In the last years, topics related to distributed generation (DG) and renewable energy sources are facing an increasing attention by the power electronics community. The recent oil cost reduction in international markets does not seem to reduce this tendency [1]. Developments in power electronic switching technologies and in DC–AC converter control techniques have been assuring a steady expansion of connections of such sources into the power grid.

One of the major applications of PLL algorithms is the synchronization of balanced currents injected by DG systems into the grid. The currents are to be synchronized with the positive sequence of the grid phase voltages at the point of common coupling (PAC) between the inverter and the mains. The currents are injected through grid-tie inverters and their control system must build current references whose phases are provided by the PLL. In addition, it is expected that the inverter control system has a measurement system able to acquire and sample the grid three-phase voltages and currents. The voltages are inputs to the PLL which is implemented in a microcontroller. The synchronization determines the amount of active power injected from the DG system to the grid. In addition, it might affect the system stability and its ride-through capability for short-duration faults [2–4].

The SRF-PLL is the most popular synchronization technique presented in the control of DGs. [5,6]. It relies on the decomposition of the three-phase voltages into synchronous voltages, v_d and v_q. This technique can also be used for single-phase PLLs, by incorporating a structure to generate voltages in quadrature from a single sinusoidal voltage [7]. However, it may be affected by harmonics contaminating the grid voltages. One solution can be the reduction of the control system bandwidth. Nevertheless, this is not efficient when it comes to low-order harmonics or unbalanced voltages, due to the production of unacceptable slow dynamic response.

* Corresponding author at: Department of Electrical Engineering, Universidade Federal da Bahia, Brazil.
E-mail addresses: luizhss@ufba.br (L.H.S. Silva), alfeu.sguarezi@ufabc.edu.br (A.J. Sguarezi Filho), darlan@cear.ufpb.br (D.A. Fernandes), fabiano.costa@ufba.br (F.F. Costa), ajmcardoso@ieee.org (A.J. Marques Cardoso).

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There are several approaches to overcome the limitations of the standard SRF-PLL. In [8], it is presented a dynamic positive sequence decoupler to be used in conjunction with the SRF-PLL. The decoupling network is able to cancel out the effect of any spurious *m*th order harmonic from the positive sequence represented in the *dq* frame. In [9], it is suggested the usage of four enhanced single-phase PLL (EPLL). Three of them are employed to provide the harmonic-cleaned three-phase grid voltages along with their 90 degrees-delayed versions. The six signals are then used to estimate the fundamental-positive sequence by means of the instantaneous sequence component (ISC) theory. The fourth PLL is applied to estimate the phase of the positive sequence.

The ISC theory allows the sequence components, originally defined in the frequency-domain, to be estimated in the time-domain. In [10], it is presented a historic overview of such strategy and it is proposed a gradient descent-based method to calculate the grid voltages instantaneous sequence components. This is accomplished by considering the relation $e^{\pm j2\pi/3} = -1/2 \pm \sqrt{3}/2e^{j\pi/2}$, that calls the need for realizing a delay of 90°. Towards this purpose, a dual second order generalized integrator (DSOGI) pre-filter to build orthogonal signals was applied in [11]. This technique is effective to attenuate second-order harmonics caused by the negative sequence component [12]. The second-order generalized integrator SOGI algorithm can be affected by harmonics and by frequency deviations [13]. Regarding, this latter distortion, an usual action is the use of a frequency-locked loop structure to supply the actual voltage frequency to the SOGI [14]. In [15], a correction of the quadrature voltages amplitude based on the frequency deviation is proposed to cancel the second-harmonic ripples in the estimated parameters of SOGI-PLLs. With regard to harmonic robustness, it is common the usage of filters to clean out harmonics presented in the quadrature voltages [16]. Another approach for constructing orthogonal signals from a single sinusoid is through the use of adaptive notch filters (ANF) [17,18]. In [17], the authors suggested to insert control loops into the DSOGI-PLL and ANF-PLL enabling them to reject the DC component. This interference might occur due to the presence of second-order harmonics across the DC inverter bus or due to saturation in the core of the voltage transformers.

An alternative strategy for extracting the positive sequence component relies on a simple averaging of $\vec{v}_{\alpha\beta}(t)$ and $\vec{v}_{\alpha\beta}(t - T/4)$ voltages, being T, the grid fundamental period. This technique is known as delayed signal cancellation (DSC) [19,20]. In [21], it is proposed a generalized delayed signal cancellation (GDSC) in which are applied four complex linear operators in series. These operators enable to eliminate all positive and negative sequence harmonics up to the 24th order. In [22], another GDSC superposition was proposed which turns the PLL algorithm robust against any arbitrary harmonic component. Recently, an improved DCS version has been proposed in [23]. In this reference, the DSC applies a moving average filter together with a phase compensator and *dq* feedback in order to reject harmonics and it has a fast dynamic response. In [24], it is proposed a combination of an adaptive DSC operator with multiple non-adaptive DSCs to serve as a preprocess stage for a PLL. In order to readjust the phase and magnitude errors caused by the non-adaptive DSC operators, a compensator is connected in series to them.

Other interesting approaches for realizing PLL algorithms are those ones based on complex-coefficient filters (CCF-PLL). This family of PLL has a fast dynamic response associated with harmonic rejection capabilities. A thoughtful discussion about this technique is presented in [25]. In [26], a proposal for enhancing the standard CCF-PLL is suggested, through the tuning of PI controllers, and in [27], a version of the CCF-PLL in the z domain is discussed. In [28], several pre-filtering methods are discussed in a complex vector perspective, and it is proposed a second and a third-order complex filters which are effective for eliminating the interference arising from the negative sequence and also for reducing higher order harmonics. Within the same theoretical framework, it is proposed in [29], an enhanced CCF-PLL based on a more effective frequency feedback from the PLL loop to the complex filter.

Differently from the aforementioned techniques which estimate the positive sequence component beforehand, an alternative strategy to enhance the SFR-PLL is to use a filter in its inner control loop to reject the harmonic interferences or voltages asymmetries, as proposed in [30]. This work presents a moving-average filter (MAF) in conjunction with a lead compensator to counteract the delayed dynamics introduced in the PLL control loop. In [31], it is introduced a MAF filter with a proportional gain component incorporated to its structure, which enables the PLL to reject low-order harmonics. This component does not add any extra delay to the PLL loop and hence does not affect the system stability.

This paper proposes a phase-locked loop scheme based on two equal blocks in series. Each block is composed of a positive-sequence estimator and the SRF-PLL. The sequence estimator relies on the description of the phase voltages in the stationary $\alpha\beta$ frame, as suggested in [32]. However, its harmonic rejection capability is improved through the usage of an one-cycle Fourier algorithm. Thus, the proposed technique is able to perform a quick and efficient filtering of harmonics of different orders besides rejecting the DC components of the voltages under analysis. Also in this paper, the cascaded blocks provide adaptability in terms of frequency deviations. The first block estimates the grid-voltages fundamental frequency. This frequency is then supplied to the second positive-sequence estimator in the second block, along with the same voltages. The frequency adaptability is a problem for PLL algorithms which rely on positive-sequence estimators such as the DSC-PLL or the DSOGI-PLL. Simulations and experimental results are provided, which show that the proposed synchronization can achieve a fast and accurate response under any grid interference or severe harmonic conditions.

2. Positive sequence estimator enhanced by the OCF filter

The proposed PLL relies on the voltage positive sequence described as follows. This estimator operates on the voltages v_α and v_β, which are extracted from the instantaneous values of the phase voltages v_a, v_b and v_c. The three-phase voltages v_a, v_b and v_c can be represented by a synchronous vector $\vec{v}_s$ in the α and β plane, whose angular velocity is ω. When the phase voltages are sinusoidal, there is only the positive sequence. Thus, ω and $\vec{v}_s$ are positive constants and $\vec{v}_s$ rotates counterclockwise. In case of any unbalance in the power grid, the vector $\vec{v}_s$ can be defined by a sum of two vectors: one of positive sequence, $\vec{v}_p$, rotating counterclockwise with velocity ω, and another of negative sequence, $\vec{v}_n$ that rotates clockwise, with angular velocity $-\omega$. Each of these vectors has constant magnitudes V_p and V_n. The angular positions are given by $\theta_p = \omega t + \phi_p$, for the positive sequence, and $\theta_n = -\omega t + \phi_n$, for the negative sequence, as can be seen in Fig. 1. Examining this figure, it is possible to write the voltages v_α and v_β as [32]:

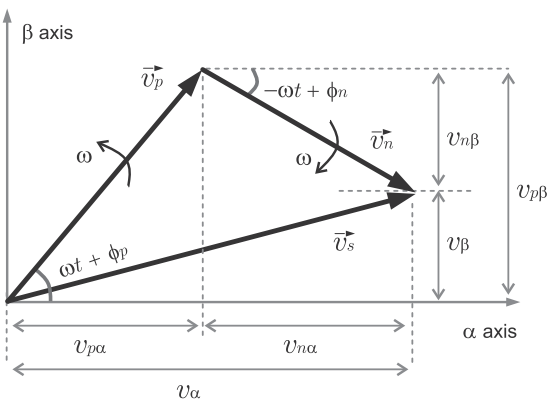

Fig. 1. Decomposition of the synchronous vector in the $\alpha\beta$ plane.