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Hybrid modeling of power electronic system for hardware-in-the-loop application

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ABSTRACT

In real-time simulation applications, hardware-in-the-loop (HIL) within nanosecond time step of large size power electronic systems involving high-frequency control strategy is still a big challenge today. In this paper, we propose a new hybrid modeling approach based on a novel nodal analysis and solving method in order to achieve both fast and accurate real-time simulation. The decoupling method allows dealing with circuit element separately regardless the size of power electronic system. After system matrix is obtained, an innovative approach using Cholesky decomposition is proposed. At last, a comparative case study of traction system in the electrical locomotive train is also presented. For this case study, implementations are made on a Field Programmable Gate Arrays (FPGA) Kintex-7 embedded in National Instruments FlexRIO PXIe-7975. Results obtained show that the proposed modeling algorithm can achieve both accuracy and efficiency within a 50 ns fixed real-time simulation time step. Besides, the comparison with results obtained from Simpower system in Matlab allows evaluating the accuracy of our proposed modeling approach.

1. Introduction

Real-time simulation is a widely used modern technique for power electronic systems design and validation [1]. Its application is mainly focused on hardware-in-the-loop (HIL) and prototyping control tests that aim at reducing the time of development and its associated cost in the controller design [2–4]. The difference is whether a physical part of the system (such as a controller or a power converter) is involved and connected to the simulation model through real input–output interfaces. Indeed, high-frequency switching devices (e.g., IGBT, MOSFET) can be commonly found in modern power electronic systems with switching frequency in a range of several kHz and up to hundreds of kHz. This generally implies that the simulation time step of a power electronic system cannot be larger than some microsecond. Thus, the particularity of real-time simulation in power electronic systems is its requirement of a tiny simulation time step to minimize the simulator latency. During the past years, the application of FPGA technologies in HIL simulators has emerged as a leading trend [5]. FPGA based simulator provides low latency and excellent computational power thus allowing a much smaller real-time simulation timestep. However, this type of simulators is mainly dedicated to limited-size power electronic systems due to the limitation of FPGA resources.

In order to increase the performance of FPGA based real-time simulators, a computationally efficient power electronic system model is apparently required. A power electronic system is distinguished by the presence of power switches (IGBT, MOSFET, etc.), which can be presented as a set of discrete systems under different switch states [6]. For modeling and simulation of a power electronic circuit, the circuit topology must be analyzed first. That means, how the circuit elements are interconnected, what are the elements constitutive, how the element terminal currents and terminal voltages are related. All these information is related to the size of the system, which is further related to the utilization of FPGA resources [7]. Due to different treatment of semiconductor switch device, there are two main modeling approaches to simulate a power electronic system in the FPGA: constant topology approach and varying topology approach.

Constant topology technology, considers the switch as a resistive device with the attempt to keep the circuit topology fixed. In addition, its solver usually combines nodal analysis or modified nodal analysis. In Ref. [8], the authors combined state-space and nodal analysis for the simulation of electrical systems. An LU factorization and a sparse matrix-based solver which is efficient for larger systems are used in the solving process. The nodal method offers the efficient solution of networks s and nonlinear functions. The drawback of this method is that it

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requires a matrix solver. How to deal with the matrix solving process in FPGA is the main hurdle in this method. In order to avoid the numeric fill-in problem caused by large size, sparse matrix, the commonly used method relies on the portioning method, which relies on the decomposition of the whole system into different subsystems [9,10]. Thus, in one time-step, only sub-circuits that have switch state changes need factorization in the matrix solver. Ould-Bachir et al. [11] proposed a network tearing technique that allows subsets of switches to be treated independently. A Gauss-Jordan processing unit is implemented to solve interface voltages/currents from the torn circuit. However, it needs a relatively long calculation time. The similar solver can be found in Refs. [12,13] to solve the multi-modular multilevel converter (MMC) for HIL application with an FPGA–CPU structure. In Ref. [14], the authors proposed a method to reduce the matrix dimension in order to solve it in real time. But it is too complex to be implemented in FPGA. On the other hand, associated discrete circuit (ADC) method is another modeling approach to keep the circuit's state-space equations fixed [15]. In Ref. [16], the authors proposed a modified ADC for the simulation to enhance the simulation accuracy. The ADC switches can greatly improve the simulation efficiency by avoiding the modification of system matrix during switching. But its convergence process causes false numerical transients thus restricts its operation at high switching frequencies. In sum, fixed matrix modeling approach could work without knowing a priori about the hybrid system before the FPGA implementation. However, the main difficulty for making such simulation in real time is due to the involved circuit size and the relatively complicate calculation steps.

By contrast, varying topology approach considers the switch as an ideal behavior and utilizes the memory unite to store all the possible equivalent circuit representations based on the combination of switches states. In Ref. [17], the authors calculated the model firstly offline and stored the results from different switch states in dedicated processor memory before FPGA implementation. Then, state-space and vector multiplication are used to solve the whole system in the FPGA. Despite this method avoids the matrix inverse process and the total simulation time can be reduced to sub 500 ns, the required memory storage is the main drawback for its implementation. When dealing with large size power electronic system, the state-space representations of variable topology method could be too large to be able to be implemented. However, when dealing with large size power electronic system, the state-space representations of variable topology method could be too large to be able to implement.

Another challenging issue regarding FPGA-based simulator is how to improve the hardware efficiency and allow efficient exploitation of the FPGA potential is also a key challenge in the HIL implementation. In the literature, the FPGA based simulation time step has been reported in the range of 500 ns–1 μs [18–22], using design Toolboxes such as System Generator in Xilinx and Hardware description language. Nowadays, high-level synthesis (HLS) tools available in the market have allowed high-level languages to design the hardware [23]. In Ref. [24], the benefits of HLS tool to develop FPGA based real-time simulator has been thoroughly evaluated. Results have shown that HLS has an advantage in time-step when circuit size is small, and FPGA clock frequency is less than 100 MHz. In Refs. [25,26], it has also suggested a small simulation step can be achieved by using HLS.

In this paper, in order to overcome the FPGA resource limitation and improve the FPGA efficiency, we extend the nodal analysis formulation to the ideal switch and propose a novel generic circuit formulation technique in the aim of reducing the calculation time of matrix inverse process. Compared to the existing matrix solver for power electronic circuits in FPGA [11,17] the main contributions of our proposed method can be summarized as follows:

1) The proposed formulation method can give a sparse and positive symmetric matrix representation of the modeled circuit. A re-ordering algorithm is also used to reduce the fill-in problem in sparse matrix decomposition.
2) Compared with LU decomposition, the Cholesky decomposition can achieve faster calculation speed. Based on that, a more computational efficient matrix solver process is achieved in the FPGA.
3) The proposed power electronic circuits modeling approach uses a fixed topology. The proposed matrix formation could consider all the combinations of circuit status without the need to store all the switch status in memory.
4) HLS tool in the Labview FPGA design software is also used to further optimize the simulation performance in the FPGA, which allows achieving sub 50 ns real time simulation time-step.

The paper is organized as follows. The modeling method for solving power electronic system is presented in Section 2. The proposed matrix solver is then given in Section 3. Section 4 presents a case study about a traction system that is commonly used in the electric locomotive train. The FPGA implementation of the case study is then presented and discussed in Section 5. Section 6 gives the conclusion.

2. Hybrid modeling of power electronic system

It is well-known that, for a power electronic circuit that contains N switching devices, the possible combination of the circuit is 2^N (For example, if $N = 10$, there are 1024 possible combination states) [27]. The circuit combination could be reduced if a circuit partitioning method is utilized. Usually, it includes two processes, partitioning and recovering of the system [28].

2.1. Circuit network partitioning

As shown in Fig. 1, network N has two sub-system N_1 and N_2. Assuming they are connected through p different inductor branches and a ground node 0, let $V_{\alpha n}$ and $V_{\beta n}$(n=1,2,...,p) denote quantities associated with these branches, as shown in (1).

$$V_{\alpha n}(t) = [V_{\alpha 1}(t), V_{\alpha 2}(t) \ldots V_{\alpha p}(t)]^T$$
$$V_{\beta n}(t) = [V_{\beta 1}(t), V_{\beta 2}(t) \ldots V_{\beta p}(t)]^T \quad (1)$$

The current vectors in these branches can be written as

$$I_{Ln}(t) = [I_{L1}(t), I_{L2}(t) \ldots I_{Lp}(t)]^T \quad (2)$$

Correspondingly, we can obtain a set of discrete inductor states with a chosen discretization method. For instance, forward Euler method with a given time step h will give the following expression for one branch:

$$I_L(t + h) = (h/L_L)*V_L(t) + I_L(t) \quad (3)$$

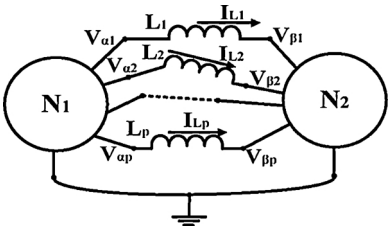

Fig. 1. Network partitioning with the inductor.