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State feedback control assisted by a gain scheduling scheme for three-level NPC VSC-HVDC transmission systems

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ABSTRACT

In this work, a feedback linearization controller together with a gain scheduling function is proposed in order to control a high-voltage direct-current transmission system (VSC-HVDC), composed by two three-phase three-level neutral point clamped converters. The described *dq0* model has the advantage of simplifying the mathematical analysis and does not disregard the zero-dynamics, against other reported solutions. In addition, based on the input-output linearization a direct current control (DCC) for the whole VSC-HVDC system is presented, where the control tasks are distributed between both converters. Moreover, a control loop to balance, in an independent way the voltage between capacitors at each converter is designed. Additionally, to the unbalance compensator, a gain scheduling scheme is proposed to assigning new tuning parameters for the PI controller, considering the system states as scheduling variables. The real-time simulator OPAL-RT® is employed as rapid prototyping and test the performance of the proposed DCC scheme.

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1. Introduction

The voltage sources converters (VSC) together with the multilevel topologies have become more popular since they provide multiple advantages for industrial applications, such as: adjustable speed drivers; uninterruptable power supplies (UPS); flexible ac transmission systems (FACTS); as well as power conversion stages in medium or high voltage direct current transmission systems (HVDC) into the electrical grids [1–3]. One of the most used multilevel array is the neutral-point-clamped (NPC) topology, where its popularity can be attributed to its low output harmonic distortion, less switching losses, high-voltage staircase-like waveform capabilities, and the ability to transfer power bidirectionally, as mentioned in [4].

However, it is worth mentioning that an inherent disadvantage of the NPC converter, is the voltage unbalance presented in the neutral point at the *dc*-link (capacitor branch) [5]. In order to overcome the above drawback, several solutions have been proposed in the literature. Some of these solutions are more focused on taking as a point of departure the power electronics developments, and others by considering a control theory approach. On the side of the electronics development, [6] shows that the voltage at the couple of capacitors in a NPC can stay balanced naturally if the control and switching signals do not posses disturbances. In spite of the fact that authors give a stability proof, it is necessary to mention that this assumption can rarely hold in a realistic scenario. Other solution consist on regulating the voltage of the capacitors in the branch by choosing a proper offset in the modulation signals, generating then a pulse width modulation (PWM) that regulates the voltage unbalance. However, the drawback of this approach, is the resulting high-switching frequency and the use of a complex double modulation [7–10]. A different possibility to keep the voltage unbalance minimized uses the space vector modulation (SVM) technique [11]. One of the advantages of the SVM technique is that it can manage NPC-VSCs with more than three voltage levels, however, the frequency based model produce a computationally complex solution when many harmonic components are taken into consideration. From the control theory approach, [12] defines the zero sequence current as a function of the capacitor voltage difference, however the manuscript does not show the performance of

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the balance algorithm, moreover the stability proof has not been presented in this work. The predictive control is other strategy to deal with the voltage unbalance at the neutral node, but the converter needs a set of signals with redundant switching states, at the same time this technique operates with high frequencies which are not suitable for high power converters, and the sudden voltage changes at the converter output increase the stress over the semiconductors [13,14]. Other works like [15], consider the unbalance as a sinusoidal disturbance, and by proposing an adaptive control algorithm the disturbance is only disregarded, in addition the NPC converter is analyzed just as a rectifier. The fuzzy logic control is a recent solution to keep the system in a specific steady-state point, where the amount of power flux does not change, and the issue of the voltage balance between capacitors is not completed solved [16].

In addition to the above proposals, several authors have been explored the input-output linearization technique (see for instance [17,18]). More precisely, [17] analyses a complex model of the NPC just as a rectifier and the system of [18] proposes using a standalone *dc* sources to introduce a zero component current to every single rectifier array. Unfortunately, these approaches are not applicable for VSC-HVDC transmission systems.

In order to solve the above problem, inspired by the approach proposed by the authors in [19], this paper considers a feedback linearization control for the currents through a VSC-HVDC transmission system. To this end, the main contribution of the present work is the rigorous analysis of the zero dynamics under ideal and realistic scenarios, showing that in both situations it is possible to ensure the stability of the closed-loop system. Such analysis is reinforced with a detailed mathematical model, and we illustrate the feasibility of the proposal scheme by means of a real-time platform in conjunction with a controller hardware in the loop, where the control signals have been generated by a *d*-space platform. The main aspects which characterize this proposal are: *the proposed scheme is developed to handle high power* dc *transmission applications; the zero sequence control is analyzed in detail, where such a control has been implemented to reduce the capacitor voltage unbalance and the effect of the grid imbalance conditions*. Furthermore, the proposed control of the VSC-HVDC transmission system is based on a direct current control (DCC) strategy, which is designed to achieve a bidirectional active power flux, to handle reactive power independently in both points of common coupling (PCC), to keep the voltage of the transmission line regulated, and to minimize the voltage unbalance between capacitors of each VSC. As a part of the control strategy a gain scheduling scheme is designed, that together with the feedback control, keep the voltage unbalance between capacitors minimized and allow the bidirectional power flux.

The remaining part of the manuscript is organized as follows: the whole VSC-HVDC transmission system is characterized, and its *abc* and *dq0* models are presented in Section 2. In Section 3, the control policy and the stability proof of the zero dynamics are explained in detail. After that, Section 4 shows the gain scheduling scheme and the *Gaussian* function to guarantee the bidirectional power flux. With the purpose of test the DCC scheme, a digital real-time simulator (DRTS) platform by OPAL-RT® is employed and the closed-loop behavior is discussed across Section 5. The last section is devoted to the concluding remarks.

2. VSC-HVDC mathematical model

The system under study is composed by a pair of symmetrical NPC-VSCs linked by a long distance *dc* transmission line, as depicted in Fig. 1. The switching functions of the semiconductor arrays are generated by a phase disposition PWM technique (PD-PWM), performing the power transmission tasks even if the line frequencies and the switching frequencies are not the same. This topology, in contrast with modular multilevel converters (MMC) has a reduced number of components (measuring, driving, semiconductors and passive elements). Also, the effects in the interconnected *ac* electrical grids due to the medium frequency of the switching signals could be mitigated by a well-designed passive filter.

2.1. *Mathematical model in the* abc *frame*

An *abc* model for the VSC-HVDC is generated based on steady-state conditions, assuming the following constraints:

- voltages and currents are balanced;
- both capacitor voltages of the branch are balanced and bounded;
- the phase leg of the converter is modeled as a three-position ideal switch;
- the transmission line losses are represented by a resistor.

The simplified electrical circuit depicted in Fig. 2 is derived by taking into account the aforementioned assumptions, where it is possible to see both *ac* electrical grids, the linking elements at each phase, the *dc* transmission line and the legs of the NPC, being substituted by simpler elements. Then, two electrical measures of the system are defined: the *dc*-link voltage (V_{dc_n}) and the voltage unbalance (ΔV_{dc_n}), as:

$$V_{dc_n} := V_{C_n^1} + V_{C_n^2}, \tag{1}$$

$$\Delta V_{dc_n} := V_{C_n^1} - V_{C_n^2}, \tag{2}$$

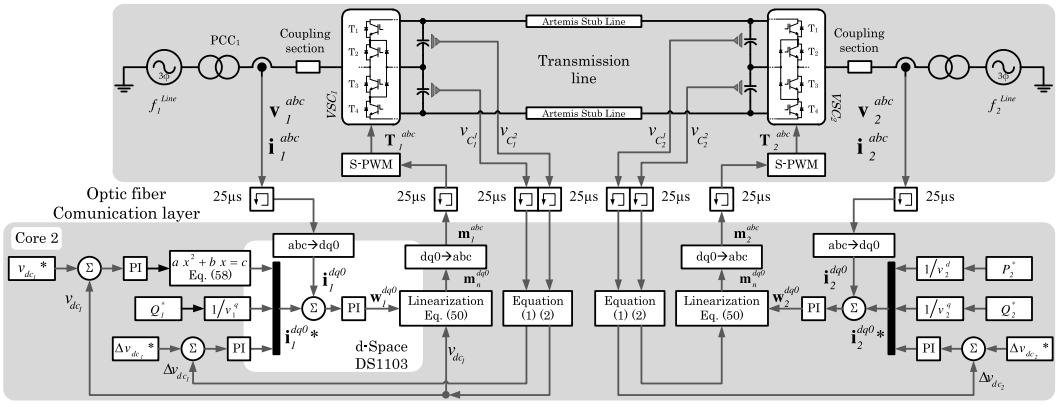

Fig. 1. The VSC-HVDC transmission system based on the neutral point clamped converter.

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