Electric Power Systems Research 155 (2018) 121–130

Contents lists available at ScienceDirect

Electric Power Systems Research

journal homepage: www.elsevier.com/locate/epsr

A method to improve the transient response of *dq*-frame cascaded delayed-signal-cancellation PLL

Menxi Xie [a], Huiqing Wen [b,*], Canyan Zhu [a], Yong Yang [a]

[a] Soochow University, Suzhou 215137, China
[b] Xi'an Jiaotong-Liverpool University, Suzhou 215123, China

ARTICLE INFO

Article history:
Received 15 May 2017
Received in revised form
30 September 2017
Accepted 4 October 2017

Keywords:
Synchronization
Phase-locked loop
Dynamic response
*dq*CDSC
Phase-lead compensator
Frequency-adaptive

ABSTRACT

The cascaded delayed signal cancellation (CDSC) based PLL in *dq* rotate frame (*dq*CDSC-PLL) can totally eliminate the disturbances of phase error. However, its open-loop bandwidth is significantly affected after incorporating CDSC into the PLL structure, so the transient response performance of three *dq*CDSC-PLLs are deteriorated. This paper proposes an improved *dq*CDSC-PLL by cascading a digital filter based phase-lead compensator into CDSC-based PLL to improve the dynamic response without sacrificing the stability. The filter shows flat gain in the passband, which can compensate the phase delay induced by CDSC and simultaneously maintain the attenuation of the notch point. The improved *dq*CDSC-PLLs significantly increases the open-loop bandwidth and enhances the dynamic performance. Besides, in order to further minimize the undesirable steady-state error, the frequency adaptive control was adopted without using any additional circuits. In order to verify the effectiveness of the proposed method, the simulation based on Matlab/Simulink is carried out for various conditions. Furthermore, experimental results for typical scenarios are provided, which highlight the advantage of the improved *dq*CDSC-PLL in terms of the dynamic performance.

1. Introduction

Grid connected power converter requires fast and precise detection of the voltage phase angle and frequency at the point of common coupling (PCC) for synchronization control. Among various synchronization methods, the phase-locked loops (PLLs) are one of the most widely used techniques. The typical structure of PLL is a closed-loop control system, consists of three major parts: a phase detector (PD), a loop filter (LF), and a voltage-controlled oscillator (VCO). Different PLL methods are proposed and characterized by different PDs, which is critical for the closed-loop control. The most popular PLL technique for three-phase system is the synchronous reference frame phase-locked loop (SRF-PLL) [1,2], which uses *Park* transformation as PD. The *q*-axis component contains the phase error information, while the *d*-axis component corresponds with the amplitude of the three-phase grid voltage. When the three-phase grid voltage is balanced and clean, SRF-PLL works well for both steady-state and dynamic due to its high bandwidth. However, power grids always suffer from all kinds of faults and disturbances, which result in serious power quality issues and abnormal states such as unbalanced, harmonic distortion, sag/swells, notches, noise, and frequency deviation. These problems could not be perfectly solved by conventional SRF-PLL since *d*-axis and *q*-axis voltage components in SRF for distorted three-phase grid voltage are no longer constant, but contain disturbances that oscillated at integer multiples of fundamental frequency considering different grid voltage scenarios. These disturbances make phase error information inaccurate, which leads to phase detection error.

To overcome this drawback, many filter techniques are applied to SRF-PLL in the last few decades [3]. It can be generally classified into two groups: out-loop filters and in-loop filters. Out-loop filters are also called the prefilter, which extract the fundamental frequency positive sequence (FFPS) from original voltage signal before feeding them into SRF-PLL. Various types of extraction methods have been discussed, such as multiple reference frame based filter (MRF-PLL) [4], three-phase EPLL [5], dual second order generalized integrator (DSOGI) [6], SVFT based filter [7], complex coefficient filter [8,9], sinusoidal signal reforming technique [10], cross decoupling in $\alpha\beta$ frame [11]. These prefilter methods improve the performance of SRF-PLL by tuning the PLL with high bandwidth. However, when the grid voltage is heavily polluted with harmonics, these methods require multiple filter units to obtain FFPS. The computational burden of these methods is high owing to the algorithm

* Corresponding author.
E-mail address: huiqing.wen@xjtlu.edu.cn (H. Wen).

https://doi.org/10.1016/j.epsr.2017.10.004
0378-7796/

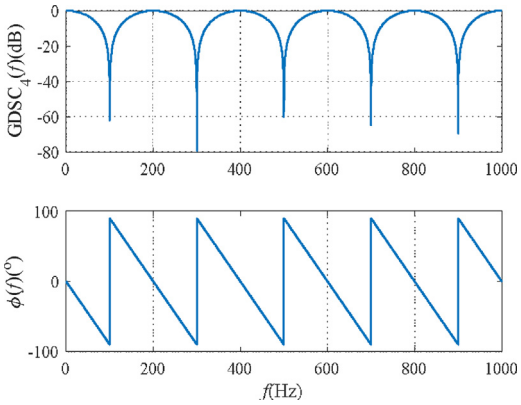

Fig. 1. Frequency response of DSC_4.

complexity. Thus, these methods are resource-consumed in practical implementation. Although the digital signal processor (DSP) becomes faster and faster, these methods are still difficult to implement considering that PLL is only a small part of the whole power converter control routine.

In-loop filters place the filter unit within the closed control loop, always before the LF [12–14]. For example, notch filter (NF) has been proposed to cancel the second-harmonic effect when grid voltage is unbalanced [12]. However, NF is not an efficient way for the distorted grid conditions since it requires cascading multiple NFs for rejecting dominant disturbances.

Moving Average Filter (MAF) has been widely used due to its convenience in digital implementation and low computational burden by circular buffer [15–18]. MAF is a linear phase filter which can be regarded as an ideal low-pass filter (LPF) if certain condition holds. It shows multi-points notch attenuation characteristics, which can completely block disturbances and leave only dc component. It is crucial to cancel the integer multiples fundamental frequency disturbances of PD even though the grid voltage scenarios are unknown. While MAF is incorporated within the SRF-PLL loop to get zero steady-state phase error under distorted inputs, additional time delay is included in the closed control loop. In order to maintain stability, the bandwidth is reduced and the dynamic performance is deteriorated [19]. Literature [20] presents a method by combing the MAF, the weighted least squares estimation, the frequency locked-loop (FLL), and the zero crossing detection to achieve a fast response, but the implementation is complicated. In this paper, a method to compensate for the phase and amplitude errors for the PMAF-PLL was proposed, which includes the SRF-PLL with MAF-based prefiltering stage. But it is only valid for limited condition.

However, since the time delay will be introduced in the in-loop of PLL inevitably, the bandwidth must be set as high as possible. Besides, in the practical design of MAF-PLL, there is only one degree of freedom, the time window length. The design flexibility is low and the dynamic response time is seriously affected especially for grid scenarios that some specific disturbances need to be selectively cancelled.

Compared to MAF, the cascaded delayed signal cancellation (CDSC) has multiple degrees of freedom and is more flexible for canceling out specific harmonic components, which depends on the grid voltage distortion [21–23]. It is another type of in-loop filter and its principle is that a harmonic can be cancelled by sum of current value and one-half cycle delayed value. Single DSC_n module can eliminate specific harmonic components while do not amplify others simultaneously. So, several numbers of DSC_n module can be cascaded together to eliminate all concerned harmonics. Furthermore, as shown in Ref. [23], MAF and CDSC are equivalent for

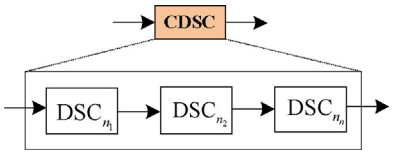

Fig. 2. Cascaded DSC*n*.

steady-state performance under certain conditions. In Ref. [23], five types of CDSC applied to SRF-PLL have been discussed according to grid voltage harmonic pattern. Because of the in-loop time delay, the CDSC based PLL gives rise to slow dynamic response of PLL, even though the bandwidth is set as high as possible. It is shown that the typical 2% setting time under phase jump of +40° is 146.2 ms (7.31 fundamental cycles). As a consequence, it will be deteriorating the entire dynamic performance of power converter.

Inspired by Ref. [24], this paper introduced a digital compensator in *dq*CDSC-PLL to improve dynamic performance without sacrificing the stability. Unfortunately, *dq*CDSC-PLL is significantly affected by the variation of grid frequency, which has to be estimated in real time by using adaptive control [25]. To address this issue, the synthesis circuit PLL was proposed in Ref. [26], which utilizes the detected amplitude and phase to generate the quadrature component. However, this method may fail when the input signal is distorted by harmonics. In Ref. [27], a stationary reference frame CDSC operator ($\alpha\beta$CDSC) was used as a prefilter for the conventional SRF-PLL. When grid frequency changes, another loop called the axis drift control was tuned to adjust the required new samples of the $\alpha\beta$CDSC blocks. However, due to high nonlinearity of the system, the model identification algorithm and controller parameter design process are rather complicated. A parallel structure presented in Ref. [22] which used one SRF-PLL to estimate the grid frequency, and then set the $\alpha\beta$CDSC filter parameter of the other SRF-PLL adaptively. Obviously, it demands more computer resources.

In this paper, a feedback frequency loop is introduced to update the buffer size of both CDSD and Cascaded Phase-Lead Compensator (CPLC). With the improved frequency adaptive *dq*CDSC-PLL, the open-loop bandwidth is increased and the dynamic performance is significantly enhanced. Furthermore, the undesirable steady-state phase error is minimized.

2. *DQ*CDSC-PLL

2.1. Phase error under distorted conditions

Phase error is the critical information for close-loop SRF-PLL, which is the output of the *Park* transform. Under the quasi-locked state, the *h*th harmonics in *abc* stationary frame correspond to (*h*-1)th components in *dq* rotate frame. When the grid voltage is distorted with odd-order harmonics, the PD output contains even-order disturbances. Specifically, the fundamental term in *abc* stationary frame corresponds to dc component in *dq* rotate frame. The phase error of FFPS is represented by the dc component, which should be kept while all the other high order disturbances should be removed out.

2.2. Delayed signal cancellation

Basic principle of delayed signal cancellation is that the sinusoidal waveform is half-wave symmetric. A harmonic can be cancelled by the sum of the current value and its one-half cycle delayed value.