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SOI-MESFET with a layer of metal in buried oxide and a layer of SiO_2 in channel to improve RF and breakdown characteristics

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ABSTRACT

A novel silicon on insulator metal semiconductor field effect transistor (SOI MESFET) structure is presented in this paper. The proposed structure includes a thin layer of nickel located in the buried oxide (BOX) of the structure which causes RF parameters to experience improved values. A thin layer of oxide in the channel under the gate edge near the drain, controls the electric field distribution and has considerable effect on the breakdown voltage. The breakdown voltage is increased by 53%. In addition, the maximum output power density is improved by 148%. The gate capacitances are reduced as a result of decreasing the depletion region extension into source and drain regions and due to the effect of metallic region in the BOX. So the proposed structure has better RF and high voltage characteristics compared to the conventional structure in terms of breakdown voltage, maximum oscillation frequency, cut-off frequency, and maximum output power density.

1. Introduction

Silicon-on-insulator (SOI) technology constitutes an important fraction of high speed and low power consumption circuits. SOI technology has many advantages such as reduced junction capacitances, latch-up immunity and improved device isolation by the use of buried oxide [1–3]. Metal-semiconductor field-effect-transistor (MESFET) is one of the most promising devices for high power and microwave circuits because it has amazing electrical and physical features including high breakdown voltage, high current density, high power density, and the capability to work at high temperatures [3–8]. SOI MESFETs are considered as reliable devices for high power and high speed applications and have many advantages over the conventional CMOS devices. CMOS technology is a low-cost technology which can be used in integrated circuits because of its ability to merge RF circuits and digital logic circuits on a single IC [2,9–11]. Although SOI MESFETs have considerable RF characteristics, some applications need higher frequency and power density. To response these demands, recently many works based on changes in the structure of SOI MESFET have been reported [8,12–16] to improve device characteristics.

Due to the trade-off between drain current and breakdown voltage, power density enhancement has been limited. It is worth to note that increasing channel doping level and channel thickness leads to drain current increment while breakdown voltage will be decreased [8]. Breakdown phenomenon occurs at the gate edge near the drain side at the surface of the device which is due to the electric field concentration [8,17–23]. Considering this issue, the challenges discussed in this paper include preventing the expansion of the depletion region toward source and drain regions, controlling the electric field, modifying channel charges and removing the gate adjacent spaces in order to increase breakdown voltage and drain current. So the proposed structure contains an insulator region in the channel which controls the expansion of the depletion region. Breakdown voltage of the presented structure is enhanced mainly because of three reasons. First, the critical electric field of the oxide is higher than silicon used in the conventional structure. Second, the oxide layer prevents the expansion of the depletion region then it requires higher drain voltages for breakdown occurrence. Third, due to the metal layer ability in dispersing the equipotential lines. So the Breakdown voltage of the proposed structure is higher than that of the conventional structure. Also, the additional layers modify the gate capacitances and consequently enhance the RF characteristics of the device. More discussions and detailed descriptions will be presented in next sections.

2. Proposed SOI MESFET structure and simulation method

Fig. 1(a) and (b) show the schematic view of the conventional and the proposed structures, respectively. Both structures contain a p-type substrate, a buried oxide (BOX), and an active layer. The difference between the structures is this point that the proposed structure includes

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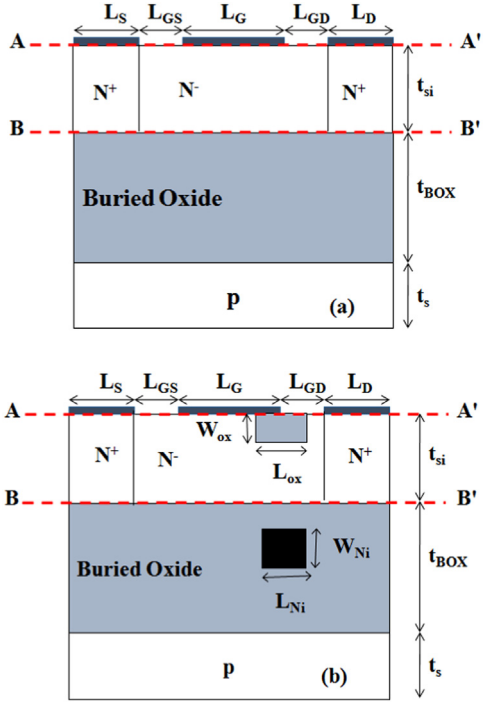

Fig. 1. Schematic view of conventional structure (a) and proposed structure (b).

Table 1
Utilized parameters for the simulation of the structures.

Device parameters	Value
Gate length	0.5 μm
Drain length	0.3 μm
Source length	0.3 μm
Gate-Drain spacing length	0.5 μm
Gate-Source spacing length	0.5 μm
Channel thickness	0.2 μm
Buried Oxide thickness	0.4 μm
Substrate thickness	0.1 μm
Source/Drain doping concentration	1e20 cm^{-3}
Channel doping concentration	5e17 cm^{-3}
Substrate doping concentration	1e13 cm^{-3}
Oxide length	0.7 μm
Oxide center distance from device left end	0.9 μm
Metal width	0.05 μm
Metal length	0.45 μm
Metal center distance from device left end	1.55 μm
Metal distance from channel	0.05 μm

an oxide layer in its channel and a metal layer in its BOX. It is worth noting that the oxide layer utilized in the channel is made of SiO_2 and the metal layer is made of Nickel. It should be mentioned that some technological problems may be occurred in using Ni as metal layer in the BOX because the nickel adherence on SiO_2 is poor. In this case, to get a good contact between nickel and SiO_2, it is necessary to deposit an adhesion layer, such as titanium. Using other materials as metal layer in the box may remove this problem but may result in other fabrication difficulties. The main role of metallic region is modifying the gate capacitances which will be discussed in next sections. We have done similar simulations for metals other than Ni as metal layer such as Al and Ti. Simulations show that for different metals the results are similar and their differences are small and can be neglected. Thus, using Ni is not mandatory and if there is a problem with fabrication, the designer can use other metals. Required parameters for the simulation of both structures are listed in Table 1. The process flow for the fabrication of the proposed structure is explained in this section too. To do that, we need two < 100 > oriented silicon wafers A and B, as shown in Fig. 2(a). Then SiO_2 is deposited on wafer A which will role as a part of the buried oxide of the transistor. The next step is via definition on the oxide in order to deposit the metal layer in the buried oxide. As can be seen in Fig. 2(d), some additional metal particles are deposited on the structure too, so performing a chemical-mechanical planarization (CMP) process is necessary in order to remove the extra metal layer. The next step to develop the proposed structure is depositing the remaining part of buried oxide. Si wafer B is considered as the handle wafer, so we need to flip the developed structure in Fig. 2(f) and then bond it to wafer B. Then the structure shown in Fig. 2(g) will be obtained. After that, another via definition is needed to be done to locate the additional oxide layer in the channel. So, after deposition of oxide and doing CMP, conventional metallization steps should be done to complete the fabrication process and achieve the structure shown in Fig. 2(k).

2-D ATLAS simulator from SILVACO software is utilized for simulating the structures [24]. ATLAS is not only associated with device layout, but also is able to analyze both DC and RF characteristics of the device. It is worth mentioning that silicon (Si) material parameters are used to simulate the structures. Also the simulator is calibrated with the experimental data from [25] and the results are shown in Fig. 3. It shows a good agreement between the simulation results of this paper with the experimental data of [25]. In order to achieve precise results, it is necessary to activate some physical models in ATLAS simulator, such as SRH: Shockley-Read-Hall (SRH) Recombination, Auger: Auger recombination model, bbt.std: standard band to band tunneling, analytic: the analytic low field mobility models, fldmob: field-dependent mobility, conmob: Concentration Dependent, Incomplete: Incomplete Ionization, and impact selb: Selberherr Impact Ionization [24].

3. DC simulation results and discussions

Fig. 4(a) and (b) show the electric field distribution of the conventional structure and the proposed structure, respectively. Electric field concentration on drain side corner of gate metal is obvious. At this region, due to high electric field, the probability of breakdown is higher than other regions. Creation of metal and oxide layers in proposed structure redistributes the field lines as shown in Fig. 4(b). Colored legends illustrate that in proposed structure, inside the oxide region, the electric field has been increased. Additional figures that zoom in on high field region help to see that electric field lines are more concentrated in oxide region of proposed structure. To more investigate this issue we have plotted Fig. 5. A comparison between the electric field of the conventional structure and the proposed structure are shown in Fig. 5. This plot is obtained through AA' cutline shown in Fig. 1, at the applied bias of $V_G = -3$ V. As mentioned before, the breakdown phenomenon occurs at the gate edge near the drain side, which is the place where the electric field focus is high. Oxide layer in drift region increases the electric field and metal layer in the BOX lowers the electric field. By considering both layers, the final electric field has been increased. Simulations show that these two layers help to increase the breakdown voltage but with two different mechanisms. In the proposed structure, by using a metal layer in the BOX and optimizing its position and dimensions, the electric field distribution in the channel is modified and redistributed such that a higher voltage is needed for the electric field to reach its critical value. Using an oxide region in the drift region increases the electric field at the gate corner but due to the higher critical field of the oxide than semiconductor, in spite of increased electric field, our proposed structure can tolerate higher fields than conventional structure. The critical electric field of Si, and SiO_2 are about 0.3 and 10 MV/cm respectively which shows about 33 times higher tolerable field in SiO_2. Also, to describe the influences of additional metal layer and oxide layer on electric field distribution and breakdown voltage clearly, the electric fields in the presence of either metal layer or oxide layer are shown in Fig. 5. It can be seen that in the presence of only metal layer, the maximum electric field