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Novel power U-MOSFET with SIPOS pillars

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ABSTRACT

In this paper, a novel vertical *U*-MOSFET using Semi-Insulating Poly-crystalline Silicon pillars (SIPOS) is presented. The proposed SIPOS UMOS combines two benefits of majority carrier accumulation and electric field modulation to improve the trade-off between the breakdown voltage (*BV*) and the specific-on-resistance ($R_{on,sp}$) of the device. In the off-state, the reshaping effect of the SIPOS pillars enhances the vertical electric field strength and weakens the peak electric field at the bottom of the gate trench, thereby increasing the *BV*. In addition, a highly doped *N*-drift is allowed for SIPOS UMOS because of the enhanced depletion by the SIPOS pillars, leading to a low $R_{on,sp}$. In the on-state, the $R_{on,sp}$ is further reduced by the majority carrier accumulation layer that formed in the drift region. The results carried by TCAD simulation show that the *BV* of SIPOS UMOS is increased by 12.5% and 36.2% compared with the conventional superjunction UMOS and the UMOS without the SIPOS pillars in the same drift length, respectively. Moreover, the $R_{on,sp}$ of SIPOS UMOS is reduced by 31.3% and 85.8%, respectively.

1. Introduction

With the advent and development of trench technology, trench gate structure *U*-MOSFETs are widely used in power supplies to achieve low conduction loss because the parasitic (Junction Field Effect Transistor) JEFT effect is eliminated and the cell size of the device is reduced [1–3]. However, for the conventional UMOS, to improve the breakdown voltage (*BV*) by increasing the drift region length (L_D) of the device and reducing the doping concentration (N_D) of the drift region, the specific on-resistance ($R_{on,sp}$) of the device increases rapidly, being limited by the silicon limit ($R_{on,sp} \propto BV^{2.5}$) [4,5]. For the purpose of breaking the silicon limit, superjunction (SJ) technology has been applied in the UMOS forming SJ UMOS. However, the SJ structure is very sensitive to the charge balance [6–10] and thus requires a highly accurate process and results in high fabrication costs. Because the drift region of SJ UMOS has a high N_D at the expense of half of the drift region width, the value of $R_{on,sp}$ is restricted. Moreover, the $R_{on,sp}$ of SJ UMOS still mainly depends on the value of N_D, which decreases with increasing *BV*, leading to SJ UMOS having a high $R_{on,sp}$ at high *BV*.

To further optimize the trade-off between *BV* and $R_{on,sp}$, a new UMOS with Semi-Insulating POly-crystalline Silicon (SIPOS) pillars is proposed (see Fig. 1(a)). For SIPOS U-MOS, two benefits of majority carrier accumulation (MCA) and electric field (*E*-field) modulation are combined to promote the trade-off between the *BV* and $R_{on,sp}$ of the device. For SIPOS UMOS, the vertical *E*-field of the device overall increases and the peak *E*-field at the bottom of the decreases via the addition of SIPOS pillars, resulting in improvement of the overall *E*-field of the device and increase of the *BV* of SIPOS U-MOS. Moreover, because of assistant depletion of the SIPOS layer, the doping concentration of the *N*-drift is increased, thereby reducing the $R_{on,sp}$ of SIPOS U-MOS. In addition, in the on-state, the value of $R_{on,sp}$ is further reduced by the MCA layer formed in the drift region.

2. Device structure and mechanism

The schematic cross-section of the proposed SIPOS UMOS is shown in Fig. 1(a). The main feature of SIPOS UMOS is the adoption of SIPOS pillars under a U-shaped gate trench of the device. The doping concentration and the width of *N*-drift region are N_D and W_N, respectively. The SIPOS layer has a width of T_S. The *E*-field in the drift region is modulated by the uniform *E*-field in the SIPOS layer according to the principle of current continuity [11]. A high *BV* is obtained via the improved *E*-field in the drift region. A higher N_D can be easier to deplete because of the enhanced assistant depletion of the adjoining SIPOS layer. In addition, an accumulation layer of majority carrier is formed in the drift region by the presence of the SIPOS layer in the on-state, thereby further reducing the value of $R_{on,sp}$. Fig. 1(b) and (c) show the cross-section of the basic cell structure for SJ UMOS and the conventional UMOS structures, respectively. In this paper, 3-*D* device simulations are conducted at room temperature. The key parameters of the optimized three UMOS structures used in the simulation are all listed in Table 1.

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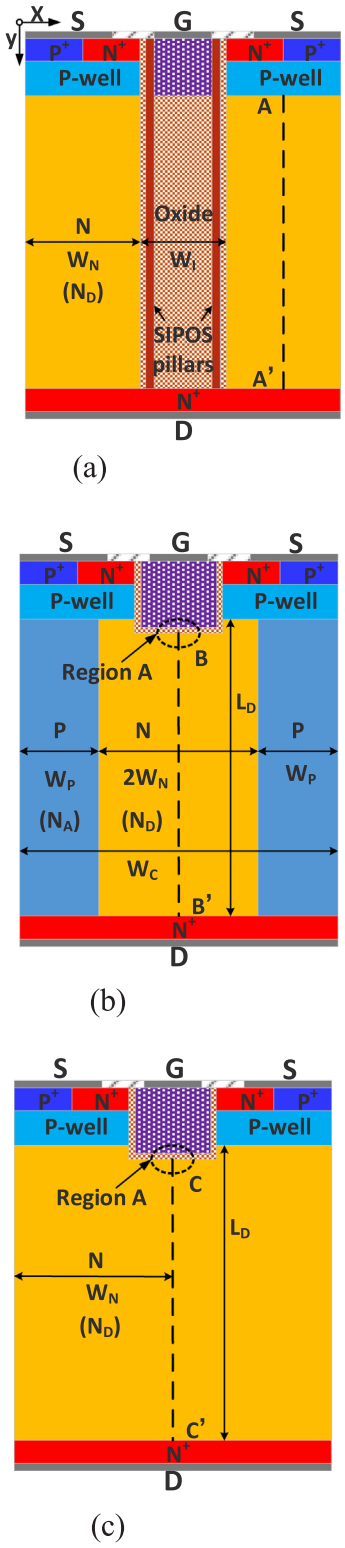

Fig. 1. Three schematic cross-sections of (a) SIPOS UMOS, (b) SJ UMOS, and (c) Conventional UMOS.

3. Results and discussion

3.1. Off-state characteristics

The bulk *E*-field distributions of SIPOS UMOS, SJ UMOS, and the conventional UMOS (along *A-A′*, *B-B′*, *C-C′*, see Fig. 1) are shown in Fig. 2. The vertical *E*-field distribution of the drift region for SIPOS UMOS is more uniform than that of the other two devices. Moreover, there are two *E*-field peaks (E_{PK}) for SJ UMOS and the conventional one at the bottom of gate trench in the oxide layer (Region *A*, see Fig. 1(b) and (c)); the presence of these two *E*-field peaks reduces the performance of UMOS. As a result, the *BV* of SJ UMOS and the conventional one is 609 V and 503 V, respectively. Because the SIPOS pillars have uniform resistivity, the fully depleted drift region in SIPOS UMOS has a uniform flat *E*-field distribution. In the off-state, there is a uniform potential difference (ΔV) between the SIPOS layer and the vertical surface of *N*-drift region (see Fig. 2(b)). Thus, the *E*-field in the oxide layer (E_{OX}) is expressed as (1).

$$E_{OX} = \frac{\Delta V}{t_{OX}} \tag{1}$$

Table 1
Parameters of optimized UMOS structures.

Symbol	Description	SIPOS UMOS	SJ UMOS	Cov UMOS
W_N	*N* drift width (μm)	3.0	2.0	3.0
W_P	*P* drift width (μm)	–	2.0	–
W_C	UMOS Cell width (μm)	6–10	6–10	6–10
W_I	Trench width (μm)	2.0	2.0	2.0
L_C	Channel length (μm)	1.5	1.5	1.5
L_D	Drift length (μm)	10–70	10–70	10–70
t_{OX}	Gate oxide thickness (μm)	0.05	0.05	0.05
N_D	*N* drift doping (cm^{-3})	5–8 × 10^{15}	6–10 × 10^{15}	3–20 × 10^{14}
t_T	Trench depth (μm)	2.0	2.0	2.0
t_P	SIPOS pillar thickness (μm)	0.5	–	–

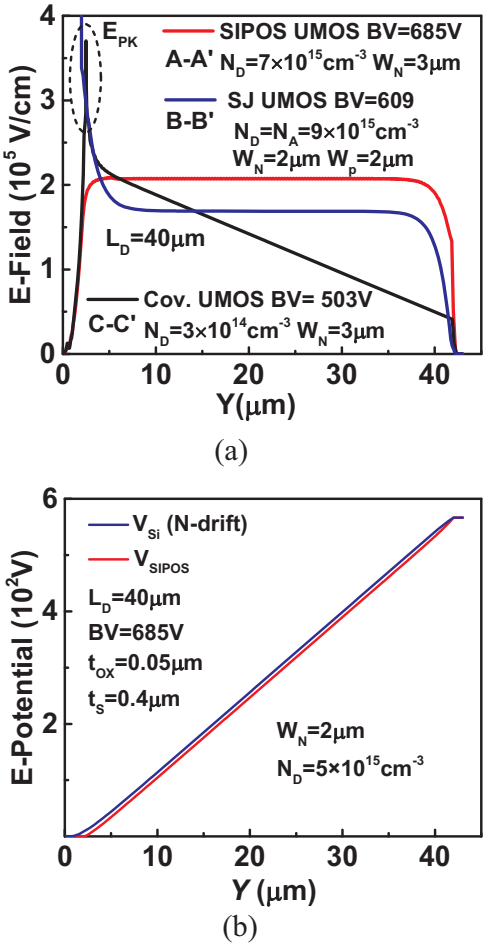

Fig. 2. (a) *E*-field distributions for the conventional UMOS, SJ UMOS, and SIPOS UMOS in the middle of the drift region; (b) electric potential difference (ΔV) between the drift region and the SIPOS pillar.