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Effect of rapid thermal annealing on bulk micro-defects and plastic deformation in silicon during high temperature processing

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ABSTRACT

We studied how rapid thermal annealing (RTA) affects bulk micro-defects (BMDs) and plastic deformation in Si wafers processed at high temperatures. BMDs caused by oxygen precipitation at 1200 °C were investigated in Si wafers as a function of annealing time with and without RTA and pre-annealing. Only the pre-annealed RTA wafer revealed an average BMD size of ~50 nm after annealing at 800 °C for 2 h and subsequently at 1000 °C for 4 h, and such wafers retained BMDs after annealing at 1200 °C for 500 min. The relationship between BMDs and plastic deformation was investigated for Si wafers subjected to RTA at various temperatures. Dislocations were generated and propagated after the simulated CMOS heat treatment as RTA temperature increased because of the low dislocation pinning effect produced by the reduction in residual oxygen while precipitated oxygen concentration increased. Incident angle deviation in the rocking curve indicated a high degree of plastic deformation caused by high RTA temperature after performing a realistic device fabrication process. We propose that a combination of RTA and a pre-annealing process can improve the internal gettering efficiency during high temperature processing, which controls BMDs. This would balance the residual oxygen and preventing plastic deformation.

1. Introduction

Controlling metallic impurities during device fabrication processes is important for reducing detrimental effects on device performance, such as leakage current, oxide breakdown voltage, and minority carrier lifetime [1–6]. Internal gettering (IG), using bulk micro-defects (BMDs) due to oxygen precipitation in a Czochralski silicon (CZ-Si) wafer, has been widely applied and is used as a metal gettering sink, has been widely applied [7–12]. BMDs contain oxygen precipitates and associated structural defects like dislocations and stacking faults. A conventional three-step thermal annealing process is used to obtain sufficient IG efficiency. High temperature above 1050 °C is used for denuded zone (DZ) formation, low temperature annealing in the 650 −750 °C range is used for nucleation, and high temperature annealing around 1000 °C is used for oxygen precipitate growth. It is also known BMDs are extremely important in silicon wafers for photovoltaics because they can provide recombination centers, which can reduce cell efficiencies [13].

However, in complementary metal-oxide-semiconductor (CMOS) processes, high temperature annealing above ~1100 °C is necessary for good drive-in. Furthermore, Si wafers continue to anneal at high temperatures up to ~1200 °C for several hours for buried layer diffusion in the bipolar processes [14]. BMDs are suppressed during high temperature due to re-dissolution of precipitated oxygen [15]. To prevent re-dissolution, BMDs must be grown to a certain critical radius before the high temperature annealing step, which can be accomplished using low-temperature annealing [16].

During the high temperature process, the Si wafer is subjected to numerous thermomechanical stresses; Plastic deformation with slip can be generated as a result [17]. Plastic deformation resistance in Si wafers is related to BMDs and interstitial oxygen concentration. However, the effect of BMDs and interstitial oxygen on plastic deformation has been ambiguous thus far [18].

Rapid thermal annealing (RTA) is also a powerful technology that is used to enhance BMDs in wafer manufacturing processes via creation of vacancies [19,20], which contribute to oxygen precipitate nucleation [21,22]. Moreover, a RTA wafer can generate uniform and high density BMDs near the surface in vacancy injection conditions, such as in N_2 or NH_3 atmospheres, where the depth profile of vacancy concentration can be controlled [23,24]. Investigations into the RTA wafers have primarily focused on the effect of RTA conditions on oxygen precipitation, interactions between vacancies and oxygen [23–25] or gettering

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efficiency throughout the wafer [26–29]. Meanwhile, the effect of RTA on BMDs near the surface and plastic deformation due to high temperature processing has not been thoroughly studied.

In this study, we investigated the effect of RTA and pre-annealing on BMDs, and the relationship between plastic deformation and oxygen precipitation, due to high temperature processing. BMDs in Si wafers with and without RTA and pre-annealing were obtained after high temperature annealing. Slip and interstitial oxygen concentration after CMOS simulation heat treatment were measured to determine the relationship between plastic deformation and oxygen precipitation. Samples were formed using a standard device fabrication process, and the wafer curvature was measured in order to validate the results after CMOS simulation heat treatment.

2. Experiment

200 mm diameter CZ-Si wafers with 725 μm thickness were prepared as samples. Surface orientations of samples were 4° off from the (100)-plane. All wafers were doped with boron. Their resistivities were in the 9–12 Ω cm range and initial oxygen concentrations ranged between 9.8×10^{17} and 12.8×10^{17} atoms/cm^3, as measured with Fourier transform infrared spectroscopy (FTIR) using a conversion factor of 4.81×10^{17} cm^{-2} (old ASTM) [30]. The concentration of substitutional carbon was less than 2.0×10^{16} atoms/cm^3 based on FTIR measurements.

The samples were divided into four groups to investigate the effect of RTA and pre-annealing on BMDs during high temperature processing, as shown Table 1. One group contained wafers subjected to RTA during the wafer manufacturing process. RTA was performed from ~1150–1250 °C for 10–30 s in a mixture of Ar and NH_3 gases, and the ramp down rate was ~30–70 °C/s. These conditions generate BMDs near the surface after moderate heat treatment. The other group contained polished wafers that were not subjected to RTA. Two additional groups contained RTA and polished wafers that were subjected to pre-annealing after the wafer manufacturing process. Pre-annealing was conducted at 800 °C for 2 h, followed by treatment at 1050 °C for 2 h in N_2 atmosphere.

Two different heat treatment procedures were performed on the RTA wafers, RTA wafers with pre-annealing, polished wafers, and polished wafers with pre-annealing. The first treatment consisted of heating at 800 °C for 2 h, followed by heating at 1000 °C for various times in an N_2 atmosphere in order to determine the effect of RTA and pre-annealing on BMD growth. The second treatment involved annealing at 1200 °C for various times, followed by a two-step annealing to generate BMDs and determine the effect of RTA and pre-annealing on dissolution of BMDs during high temperature annealing. The two-step annealing process for generating BMDs was performed at 800 °C for 2 h, followed by annealing at 1000 °C for 8 h in an N_2 atmosphere.

BMD density and size were measured with a scanning infrared microscope (SIRM) that can be used to measure the depth from the surface [31]. Here, BMD size is defined by particle contrast corresponding to the amount of light scattered from oxygen precipitates and associated structural defects, such as dislocations and stacking faults. Data was collected at 20 mm intervals in the radial direction and from the surface to 150 μm depth at each position. Data are reported as averages.

Table 1
Heat treatment condition of sample groups.

Group	Pre-annealing		RTA	
	Temperature (°C)	Time (s)	Temperature (°C)	Time (h)
No. 1	–	–	1150–1250	10–30
No. 2	800/1050	2/2	1150–1250	10–30
No. 3	–	–	–	–
No. 4	800/1050	2/2	800/1050	2/2

Table 2
Process conditions for the simulated CMOS heat treatment.

Step number	Temperature (°C)	Time (min)	Ambient
1	650	10	O_2/N_2
2	1100	20	N_2
3	650	90	N_2
4	750	30	N_2
5	800	10	N_2
6	1000	55	N_2
7	1150	260	N_2
8	800	10	N_2
9	1150	50	N_2
10	800	30	N_2
11	1000	250	N_2
12	950	10	N_2

To evaluate the gettering efficiency during the high temperature process, the RTA wafer, RTA wafer with pre-annealing, polished wafer, and polished wafer with pre-annealing were subjected to annealing at 1200 °C for 500 min. Then, 1000 ppm Cu, Fe, and Ni in 3 μL etching solutions were adhered as droplets to the backside of each wafer, and dried. Contaminated wafers were annealed at 1000 °C for 30 min so that the contaminant could sufficiently diffuse into the bulk. Subsequently, the haze, caused by an accumulation of etch pits, was inspected under high intensity light after Wright etching of the (100)-surface for 5 min. The etch pit on the wafer surface is due to outdffisuion and precipitation of metal impurities on the surface during the cooling process if gettering sinks are poor within the bulk [32].

The relationship between plastic deformation and oxygen precipitation were investigated using RTA wafers subjected to various RTA temperatures during the wafer manufacturing process. This results in different levels of interstitial oxygen after heat treatment, which generates BMDs and thermal stress. To adequately represent the complicated realistic high-temperature CMOS process, a CMOS simulation heat treatment was developed, as shown in Table 2. In an attempt to control heavy thermomechanical stresses due to temperature changes, the ramp up and down rates during CMOS simulation heat treatment were 12 °C/min and 8 °C/min, respectively.

To evaluate the tendency of slip generation during the CMOS simulation process as a function of interstitial oxygen concentration, slip dislocations were measured by X-ray topography (XRT). XRT measurements revealed that imperfections in the crystal lattice were observed only in the wafer center if plastic deformation occurred during simulated CMOS heat treatment. To show the slip generation tendency, etch pits were observed using an optical microscope after Wright etching for 5 min of the (110)-cleaved plane in the wafer center. Wright etching is a solution for preferential defect etching in silicon crystals. The solution is composed of 13–15% HF, 10% HNO_3, 13–15% CrO_3, 2% $Cu(NO_3)_2$, and 20–21% CH_3COOH [33]. Interstitial oxygen concentration, corresponding to wafers at each RTA temperature, was measured using FTIR before and after the CMOS simulation heat treatment, and the precipitated interstitial oxygen was calculated from the difference between the initial and residual interstitial oxygen.

The results after applying the simulated CMOS heat treatment were validated using RTA wafers that were processed for device fabrication, i.e., subject to RTA at 1170 °C and 1215 °C. The wafer curvature was measured using a high resolution X-ray diffractometer (HRXRD) to determine the degree of plastic deformation after a realistic device fabrication process [34].

3. Results and discussion

3.1. Effect of RTA and pre-annealing on BMDs

As described previously, RTA and pre-annealing can affect the nucleation and growth of BMDs. Fig. 1 shows the BMD density measured