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Optimization of nanometer bulk junctionless Trigate FET using gate and isolation dielectric engineering

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ABSTRACT

In this paper, the performance of bulk junctionless trigate FET is enhanced by optimizing the (WF_{ISO}) $Gate_{ISO}$ work function ($Gate_{ISO}$ is the portion of the gate above isolation dielectric), isolation dielectric permittivity (K_{ISO}), and $Gate_{FIN}$ dielectric ($Gate_{FIN}$ is the portion of the gate covering the fin) permittivity(K_{FIN}). SiO_2, Si_3N_4 and HfO_2 dielectrics with gate work functions in the range of 4–5.6 eV are used in this study. The performance is enhanced in terms of I_{ON}, I_{OFF}, $\left(\frac{I_{ON}}{I_{OFF}}\right)$ ratio, and f_T. High K_{FIN} brings up all the above parameters. While high K_{ISO} is preferred for better I_{ON}, I_{OFF}, and $\left(\frac{I_{ON}}{I_{OFF}}\right)$ performance, low K_{ISO} is improves f_T. Moderate WF_{ISO} is suggested to improve $\left(\frac{I_{ON}}{I_{OFF}}\right)$ ratio.

1. Introduction

Halo doping, Super steep retrograde channel doping, shallow source-drain extensions, high-K dielectric replacing the gate oxide, and metal gates instead of poly gates are some of the techniques to mitigate the short channel effects (SCE) faced by the conventional planar single gate MOSFET [1–6]. Building devices on Silicon on Insulator (SOI) substrate instead of bulk Silicon substrate, and mechanically stressed substrates are also some of the solutions [7,8]. Multigate structures like double gate FinFET, triple gate, quadruple gate, nanowires and nanotubes are some alternate advanced solutions to overcome the SCE [9]. Among these structures, FinFET is a potential alternative to the conventional planar structure [10–12].

From the fabrication point of view, junctionless structures have more scope at lower dimensions. Junctionless concept was introduced as trigate structure by Collinge et al., and had the source, channel and drain of the same doping species [13]. This solves the need of high doping concentration gradient in the junctions and thereby the annealing cost. Also the junctionless devices are not plagued by the surface scattering issue which is rampant in the junction based devices owing to the bulk mode of transport in junctionless devices. Similar to CMOS devices, the multi gate structures may be fabricated either on SOI or on bulk substrate [14,15].

While bulk CMOS devices use field oxide in the fabrication the bulk FinFET/trigate devices use field and isolation oxides [16,17]. While field oxide is sitting between two different devices the isolation oxide is sitting within the same device.

Fig. 1(a) shows (i) $Gate_{FIN}$, the portion of the gate running over the fin, and (ii) $Gate_{ISO}$, the portion of the gate running over the isolation dielectric. The dielectrics sitting below $Gate_{FIN}$ and $Gate_{ISO}$ have permittivity of K_{FIN} and K_{ISO}, respectively. Similarly the gate electrode work functions associated with the $Gate_{FIN}$ and $Gate_{ISO}$ are WF_{FIN} and WF_{ISO}, respectively.

We can improve the leakage current (I_{OFF}), on current (I_{ON}) and $\left(\frac{I_{ON}}{I_{OFF}}\right)$ ratio performance of the FinFET/trigate structure through optimal selection of K_{FIN}, K_{ISO}, and WF_{ISO}. Since the junctionless devices are claimed to have smaller ON currents compared to its junction-based counterpart [9] the above study would be more relevant for the junctionless devices.

The usage of high K dielectrics is investigated in the literature for MOSFETs, FinFETs and junctionless transistors [18–21]. The same holds good for the work function engineering i.e. using metals for gates [22,23]. But, the usage of high K dielectric in the isolation dielectric region of bulk trigates/FinFETs is yet to be explored. Similarly dual metal gate work function technique is reported to improve the performance of the conventional planar FET devices [24]. But, this technique is not investigated in the isolation region of the bulk trigate/FinFET structures. In essence, the isolation region of the bulk trigate/FinFET structure is yet to be analyzed for performance enhancement.

In this work, we have enhanced the performance of the bulk junctionless trigate device using the above technique, and the same has

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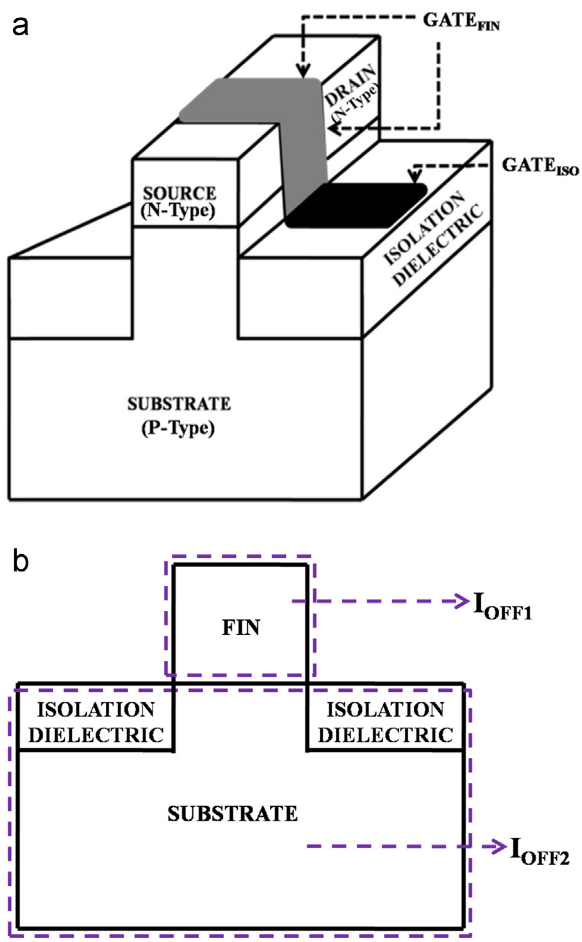

Fig. 1. (a). Schematic of Bulk junctionless Trigate FET with the N-Type doped fin.(b). Schematic of Bulk junctionless Trigate FET with cut taken at centre of the fin.

been applied on the junction-based counterpart at the end of the study. This paper is organized into nine sections. Section 1 is the introduction and Section 2 deals with the proposal to minimize leakage current. Section 3 deals with the methodology, device structure and I_D-V_G calibration. Section 4 discusses the effect of WF_{ISO} in equilibrium, ON and OFF states. Section 5 deals with the effect of K_{ISO} on the currents. Section 6 discusses the effect of K_{ISO}, K_{FIN} and WF_{ISO} on both DC and AC parameters. Section 7 deals with the analysis of leakage current in bulk junctionless Trigate FET. The effect of K_{ISO}, K_{FIN} and WF_{ISO} on the DC parameters is studied in case of inversion based Trigate FET in Section 8. Finally the Conclusion section concludes this paper.

2. Proposal to minimize leakage current

As already stated, the gate in a FinFET/Trigate with multiple fins has two different parts, (i) $Gate_{FIN}$, the portion of the gate covering the fin, and (ii) $Gate_{ISO}$, the portion of the gate above isolation dielectric, as shown in Fig. 1(a). While the $Gate_{FIN}$ interacts with the N type doped fin, the $Gate_{ISO}$ interacts with the P type doped substrate. So, this leads to two different leakage paths from drain to source as shown in Fig. 1(a) which can be categorized into,

(i) Fin region contributing to I_{OFF1}(Refer Fig. 1(b))
(ii) All regions excluding Fin region contribute to I_{OFF2}

(I_{OFF1} + I_{OFF2}) gives the device's I_{OFF}(Refer Fig. 1(b))

As already stated K_{FIN} strongly controls the fin region whereas K_{ISO} and WF_{ISO} mostly control the substrate beneath the isolation dielectric. So we hypothesize that the I_{OFF2} can be reduced without sacrificing I_{ON} significantly i.e. better $\left(\frac{I_{ON}}{I_{OFF}}\right)$ ratio can be achieved through optimization of K_{ISO} and WF_{ISO}.

3. Methodology, device structure and I_D-V_G calibration

Sentaurus TCAD simulator from Synopsys is used to perform the simulations. Sentaurus structure editor is used to create the device structure and to generate mesh for device simulation. Sentaurus device simulator is used to perform the DC and AC device simulations. Physics section includes appropriate models for doping dependency on mobility, effect of high and normal electric fields on mobility and velocity saturation.

The physics models used in the device simulation are Shockley–Read–Hall (SRH) recombination model, extended Canali model and Lombardi model [13]. The drift diffusion mechanism based simulations have been carried out. The fitting parameters for the models used is given as below:

SRH recombination model:

$$\tau_{dop}(N_{A,0} + N_{D,0}) = \tau_{min} + \frac{(\tau_{max} - \tau_{min})}{1+\left(\frac{N_{A,0} + N_{D,0}}{N_{ref}}\right)^{\gamma}},$$

where

$\tau_{min} = 0$ s, $\tau_{max} = 1 \times 10^{-5}$ s for electron and $\tau_{min} = 0$ s, $\tau_{max} = 3 \times 10^{-6}$ s for hole, $\gamma = 1$, $N_{ref} = 1 \times 10^{16}$ cm^{-3}.

Extended Canali model:

$$\mu(F) = \frac{\mu_{low}}{\left[1+\left(\frac{\mu_{low}F_{hfs}}{v_{sat}}\right)^{\beta}\right]^{1/\beta}},$$

where

μ_{low} is the low field mobility,
β is the temperature dependant parameter,
ν_{sat} is the saturation velocity,
F_{hfs} is the driving field.

Enhanced Lombardi model:

$$\frac{1}{\mu} = \frac{D}{\mu_{ac}} + \frac{D}{\mu_{sr}}$$

$$\mu_{ac} = \frac{B}{F_{\perp}} + C\left(\frac{N_{A,0} + N_{D,0} + N_2}{F_{\perp}^{1/3}\left(\frac{T}{300K}\right)^{k}}\right)$$

and

$$\mu_{sr} = \left(\frac{(F_{\perp}/F_{ref})^{A*}}{\delta} + \frac{F_{\perp}^{3}}{\eta}\right)^{-1}$$

where,

$B = 3.6 \times 10^{7}$ cm s^{-1}, $A = 2.58$, $C = 1.7 \times 10^{4}$ $cm^{5/3}V^{-2/3}$ s^{-1}, $D = \exp -^{x/lcrit}$, where x is the distance from the interface and $l_{crit} = 10^{-6}$ (cm), $\eta = 1.0e^{300}V^2$ cm^{-1} s^{-1}.

The dimensions of the bulk junctionless Trigate FET is given in Table 1. It should be noted that there is no differentiation between K_{FIN} and K_{ISO} in the calibrated device i.e. both use SiO_2. The schematic of bulk junctionless Trigate FET along the $Gate_{ISO}$ (gate running over the isolation dielectric) and $Gate_{FIN}$ (gate enclosing the fin region) is displayed in Fig. 1(a) and the corresponding 2D schematic for the device with the cut taken at centre of fin is displayed in Fig. 1(b). The TCAD

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