Materials Science in Semiconductor Processing 82 (2018) 9–13

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Effects of high in-situ source/drain boron doping in p-FinFETs on physical and device performance characteristics

Shashidhar Shintri*, Chloe Yong, Baofu Zhu, Shayan Byrappa, Bianzhu Fu, Hsien-Ching Lo, Dongil Choi, Venkat Kolagunta

GLOBALFOUNDRIES, US, Inc., 400 Stone Break Rd Extension, Malta, New York 12020, USA

ARTICLE INFO

Keywords:
SiGe epitaxy
Boron doping
FinFET
Device simulation
MOSFET
CMOS

ABSTRACT

In this study, the effects of high *in-situ* boron (B) doping in embedded source/drain (S/D) silicon germanium (SiGe) stressor of p-channel Fin Field Effect Transistors (FinFETs) in a 14 nm technology node were investigated. The device results were correlated to physical characteristics of B doped S/D regions which were probed using Transmission Electron Microscopy (TEM), Electron Energy Loss Spectroscopy (EELS) and Low Energy Electron Induced X-ray Emission Spectroscopy (LEXES) on representative device structures. B doping was established to be around low-E20 atoms/cm^3 range as measured by LEXES. Reduction in on-state resistance (R_{ON}) and an increase in drive current (I_{ON}) was observed with higher B doping in SiGe but physical constraints, especially B segregation offered manufacturable challenges. These observed results are expected to critically help in SiGe stressor based S/D junction optimization of advanced FinFET Complementary Metal-Oxide-Semiconductor (CMOS) devices.

1. Introduction

Selective epitaxy growth is a critical element in the development of Complementary Metal-Oxide-Semiconductor (CMOS) transistors in advanced nodes, including Fin Field Effect Transistors (FinFETs). Primarily, the application of selective epitaxy is for growing stressor materials in the source/drain (S/D) regions which increases channel mobility resulting in higher performance. Integrating high quality selective epitaxial films of desired doping profile is challenging since the growth is strongly influenced by factors such as incoming substrate profile, local pattern layout (micro-loading) as well as the characteristics of the dielectric films used in the process flow. [1–4]. Currently, *in-situ* boron (B) doped silicon germanium (SiGe:B) is still the preferred material of choice for pFET embedded S/D epitaxy in advanced FinFETs for achieving low sheet resistance S/D regions and for imparting the desired compressive strain in the channel [5,6]. Increasing B doping in SiGe is known to lower the on-state resistance (R_{ON}) which is beneficial for achieving higher device performances [7]. However, previous reported works on the effects of high B doping (> 1E20 atoms/cm^3) in S/D regions of FinFETs on both the physical and device characteristics are very limited [4,8], especially for Ge content over 40% in SiGe. This work presents an evaluation of modulating *in-situ* B doping in S/D SiGe:B of FinFETs on physical and device performance, till we observe the onset of increased interface B segregation during epitaxy.

2. Experimental details

The experiments performed in this work were carried out on FinFET structures on 12-in. Si wafers in the process flow of a high performance 14 nm FinFET node manufactured at the GLOBALFOUNDRIES. Fig. 1 shows a schematic fin cut cross-sectional diagram of partially fabricated pFET structures, depicting typical features on the patterned substrate such as trench isolations, embedded SiGe:B on fins wrapped by a dummy poly gate stack with side walls covered by desired spacer material. SiGe:B was grown in the recess S/D cavities using an AMAT Centura® reduced-pressure chemical vapor deposition (RP-CVD) reactor. Typically it consisted of few optimized layers which included the main SiGe:B layer (bulk of the growth). The layers were grown by grading Ge% to accommodate the strain without the generation of crystal defects. Similarly B doping is optimized (usually going from low to high with growth) to achieve desired device characteristics. The initial layer is typically a conformally grown SiGe layer with Ge% around mid-30% range and the final thin (< 3 nm) Si cap layer with B doping around 10^{18} atoms/cm^3. The main layer was grown at temperatures in the range of 550–675 °C. Post epitaxial deposition, the wafers underwent S/D dopant activation anneal followed by subsequent integration of the gate stack materials. Finally middle-of-line contacts (not shown in Fig. 1) were created to connect the devices to the backend-of-line circuitry.

* Corresponding author.
E-mail address: shashidhar.shintri@globalfoundries.com (S. Shintri).

https://doi.org/10.1016/j.mssp.2018.03.007
Received 2 December 2017; Received in revised form 29 January 2018; Accepted 2 March 2018

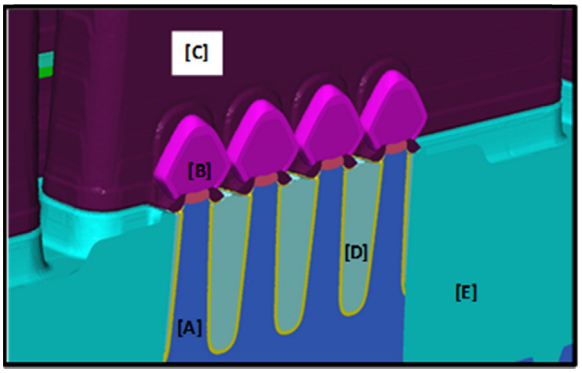

Fig. 1. Schematic cross section (cut across fin) of partially fabricated pFET structures with some key elements highlighted: [A]: Fin. [B]: SiGe:B. [C]: Gate covered by spacer material. [D]: shallow oxide trench isolation [E]: Deep oxide trench isolation.

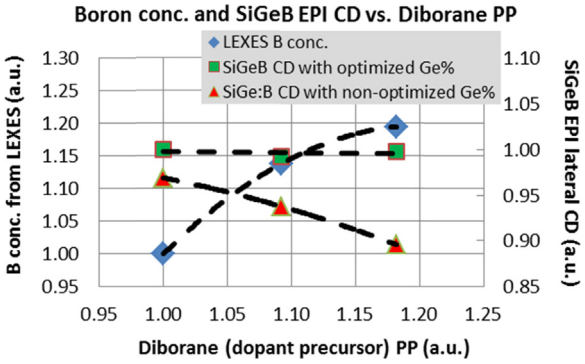

Fig. 2. Normalized values of average B doping content (from LEXES) and SiGe:B EPI lateral CD (from SEM) *vs.* 3 different values of Diborane precursor PP conditions used during S/D epitaxy.

The main focus of this work was to investigate the physical and electrical responses of changing B doping concentration in the S/D regions during selective main layer SiGe:B epitaxy. B doping modulation was achieved by changing the partial pressure of the doping precursor (2% Diborane in H_2) inside the chamber and optimizing the growth processes to keep the Ge content and selectivity nearly constant in the deposited films. Typical flow rates of Diborane used in the current study was in the range of 200–400sccm. Inline detection and quantification of B doping in finned patterned structures is generally challenging and the method that was employed at the time of the current study was Low Energy Electron Induced X-ray Emission Spectroscopy (LEXES). LEXES measurements were performed on patterned wafers and B concentration was quantified based upon the establishment of the correlation of LEXES measured data to more widely used Secondary Ion Mass Spectroscopy (SIMS) measurements performed on non-patterned wafers having a wide range of B doping in SiGe:B films. Inline LEXES measurements for this study used current of around 10 μA and a Lanthanum Hexaboride (LaB_6) tip for generating low energy electron beam with a diameter anywhere between 5 μm and 100 μm. A major advantage of this technique is that it is non-destructive in nature and is able to measure the total dopant concentration across the entire wafer that could be correlated to SIMS. Select wafers were further analyzed using Transmission Electron Microscopy (TEM) and Electron Energy Loss Spectroscopy (EELS) in an effort to analyze the physical characteristics of SiGe:B in the S/D cavities. Cross-sectional TEM samples were prepared by *in-situ* lift-out of a wedge from the wafer, followed by Focused Ion Beam (FIB) ion milling to thin the sample to make electron transparent in FEI SEM-FIB dual beam. TEM imaging and EELS analysis were performed in FEI aberration corrected Titan, operated at 200 keV.

3. Results and discussions

3.1. Physical characterizations

LEXES is a surface analytical technique that can be employed to quantify B incorporation in patterned structures with good sensitivity and repeatability. It should be noted that LEXES measured values include active and as well as non-active B species. We observed that the Ge content in SiGe played a critical role in achieving desired B doping profile. Maintaining high selectivity and uniform growth rate was a challenge and typically, increasing Ge% within a desired range helped in achieving larger and uniform EPI growth volume. Once a Ge value was set, other chamber variables like HCl gas and temperature were proportionally adjusted with increasing Diborane flows. Fig. 2 shows the normalized average values of EPI lateral critical dimension (CD) as a function of different dopant precursor partial pressures (PPs). This CD is the top-down width of SiGe:B growth seen in Fig. 1, as measured by scanning electron microscope (SEM). Typically, the CDs are sub-50 nm in size and constrained by cavity dimensions as well as device design requirements. EPI CDs at two different values of Ge% are compared here, one with non-optimized Ge% and one after Ge% optimization (latter having higher Ge% than the former). Growth recipes were optimized to keep Ge% in the different wafers nearly constant (as verified by film growth on non-patterned wafers and LEXES Ge dose on patterned structures). B doping concentrations were typically in the range of 1.6–1.9 E20 atoms/cm^3 for wafer samples tested in this study. As observed, the EPI CD showed a significant drop in growth volume at higher B doping with non-optimized Ge%, which is attributed to undesired B surface segregation resulting in degraded epitaxial growth. Rest of the work reported here was carried after ensuring the EPI CDs were nearly constant by optimizing Ge% (in the B doping range studied) around low-40% range. Fig. 2 also shows the variation of B doping measured on representative finned structures on the patterned wafers.

Cross-section TEM images on select samples are shown in Fig. 3(a-c) as a function of varying B doping levels. At higher levels of Diborane PP during epitaxy, it was observed that B tends to segregate preferably near the growth termination of the main SiGe:B layer along the {111} faceted planes. This was confirmed by TEM and EELS measurements carried on certain device structures as shown in the Fig. 3(d) on the wafer with the highest B concentration in this study. This offers manufacturable challenges as B pile-up is found to significantly contribute towards degraded and abnormal epitaxial growth and in extreme cases, wafer yield loss. In this study, Ge in SiGe:B was in low-40% range. Typically, higher levels of Ge favors reduced B segregation and lattice diffusion when films are in compressive stress [9]. However, beyond a certain limit of Ge, crystal defects resulting in strain relaxation occurs. We also observed that the growth and coverage of a lightly doped Si:B layer which was subsequently grown on the main layer was poor and less predictable at the onset of B pile up (also qualitatively seen in Fig. 3(a-c)). B segregation thus tends to affect the epitaxial quality of SiGe:B thereby preventing the nucleation of a uniform Si/SiGe layer. This optimization of kinetics between B and Ge incorporation was a critical part of this work which helped ensure that the gains from increasing B are not negated by the increase in contact resistance resulting from degraded EPI growth volume.

3.2. Simulation and device characterizations

In this study, we carried out Technology of Computer Aided Desgin (TCAD) device simulations on Sentaurus Workbench (product of Synopsys) using an up-to-date simulation deck. From the simulations it was found that the total R_{ON} of the pFET device comprised of several factors, with channel resistance (R_{CH}) dominating nearly half of it (~51%), while the remaining critical elements, lumped together as