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Crystalline phase dependent electrical properties of Mg incorporated tetragonal phase stabilized ZrO_2 high-κ dielectric layer in Si based MOS capacitors

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ABSTRACT

Electron beam evaporated Mg doped ZrO_2 (Mg:ZrO_2) high-k thin films on p-type Si(100) substrate and their metal oxide semiconductor (MOS) capacitors were structurally and electrically studied. Thicknesses of the dielectric films were in the range from 85 to 240 nm with RMS roughness between 1.4 and 2.3 nm. The targets for e-beam evaporation were made with well characterized pure ZrO_2 with monoclinic phase and with 3%Mg doped tetragonal phase stabilized ZrO_2 nanopowders. Structural phase analysis revealed that the phases of Mg:ZrO_2 thin films deposited have retained their respective phases of zirconia targets used. The incorporation of Mg ions in ZrO_2 dielectric gate layer had increased the width of the hysteresis window in the C-V characteristics. Various leakage current conduction mechanisms in the accumulation region of the MOS capacitors have been used to understand the leakage current mechanism and found that traps present in the oxide layer played a major role in explaining the leakage current. In particular, the conduction mechanisms such as Poole-Frenkel emission, Space Charge Limited Conduction and Trap-assisted tunneling were found to be dominant in these devices. A high dielectric constant of 28.9 was achieved in the Mg doped tetragonal phase stabilized ZrO_2 gate oxide films with a leakage current density of 3.32×10^{-6} A/cm^2 at − 1 V. Hence, the tetragonal phase stabilized Mg:ZrO_2 gate oxide layer showed improved electrical characteristics making them potential for memory storage devices.

1. Introduction

For the last few decades, scaling down of Complementary Metal-Oxide-Semiconductor (CMOS) devices in Ultra Large Scale Integration (ULSI) technology is in high demand. These micro- and nano-electronic MOS devices mainly depend on SiO_2 as gate dielectric oxide. In the process of miniaturization of the electronic devices, thickness of these gate oxide films has gone down to a few nm and in many cases to a sub-nm level. At this condition, the problem with the SiO_2 is its higher leakage current. In order to have a low leakage at very low thickness new materials are in need. There are many studies going on to replace SiO_2 with high-dielectric constant (high-κ) materials such as HfO_2 [1,2], Al_2O_3 [3], HfON [4], etc., in silicon based CMOS devices. Still there is a lot more research is required in order to identify new high-κ materials of required properties in the place of SiO_2. There are totally six criteria [5,6] for a material to be chosen as an alternative for replacing SiO_2 in Si based CMOS devices: (i) high dielectric constant, (ii) thermal stability with silicon, (iii) kinetically stable at high temperatures above 1000 °C, (iv) high band offsets greater than 1 eV, (v) formation of good electrical interface with Si, and (vi) presence of electrically active defects. Zirconium oxide (ZrO_2) is one of the high-κ materials, satisfying the above six criteria [7,8], it could serve as an alternative material for SiO_2 in metal-oxide-semiconductor (MOS) technology. Thin films of zirconia have been studied intensively in microelectronics such as in memory storage applications [9,10], gate dielectric materials for resistance switching [11,12] and MOS devices [13,14]. Loss due to interfacial layer and parasitic effects arising due to imperfect back contact, series resistance and wire connections must be taken care for the better performance of the device [15]. Roughness in the dielectric layer is also an important factor that could cause frequency dispersion in the capacitance-voltage (C-V) characteristics [16].

Another important factor that determines the performance of the device is the crystal structure of the gate oxide materials. The crystal structure of the high-κ dielectric thin films can alter the electrical properties of the memory devices [17]. Yoo et al. [18], have studied the effect of crystalline phases on electrical properties such as dielectric

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constants and leakage current densities of aluminum doped HfO_2 and ZrO_2 thin films in high voltage devices. They have reported that the dielectric constants of the films with amorphous and monoclinic phases of ZrO_2 were in the range of 20–25, whereas the same for ZrO_2 with cubic/tetragonal phases were in the range of 30–35. Leakage current density was the lowest for the thin films having cubic/tetragonal phase. Wu et al., reported that the dielectric permittivity (κ) of 36.2 has been achieved for the tetragonal stabilized ZrO_2 with embedded Ge nanocrystals [19]. Zirconia normally exists in monoclinic phase at room temperature but undergoes martensitic phase transformation at about 1200 °C to tetragonal structure and further transforms into cubic structure above 2370 °C [20]. However, by doping with aliovalent cations such as Na^+, Al^{3+}, Mg^{2+}, Ca^{2+}, and Y^{3+} can stabilize the cubic/tetragonal phase of zirconia. Dimri et al. [21] have optimized the cubic phase stabilized zirconia by doping Ca, Y and Mg with heat treatment above 1200 °C. Stabilizing tetragonal phase in ZrO_2 nanopowders and achieving the same crystalline properties in the thin films is a quite challenging task. By having this motivation, in this work, Mg ions were chosen to stabilize the tetragonal phase in ZrO_2 with an optimum doping content and heat-treatment conditions. The phase was stabilized in ZrO_2 nanopowder which was later made into a target for thin film (gate oxide) deposition on Si(100) substrate. The metal-oxide-semiconductor devices were made with ZrO_2 having monoclinic and tetragonal stabilized phases. Structural phase dependency on the electrical properties of the MOS capacitors is reported.

2. Experimental

Thin films of Mg ions doped zirconia (Mg:ZrO_2) were deposited by using electron beam evaporation technique. The target for the electron beam evaporation process was prepared as pellet by uniaxially pressing the Mg:ZrO_2 powders synthesized by co-precipitation method [22]. A detailed description of synthesis procedure of the powder is presented in the Supplementary information. The optimized tetragonal phase stabilized zirconia powder sample with the lowest doping concentration of 3 mol% Mg ions annealed at 600 °C has been used for the thin film deposition.

2.1. Deposition of thin films

Thin films were deposited by electron beam evaporation using a vacuum coating unit, (Model: 12A4D, Make: Hind High Vacuum Pvt. Ltd., India). The pellets of Mg:ZrO_2 nanoparticles were used as target materials. The pellets were pressed at 3 t pressure by a motorized pellet press (Kimaya Engineers, Pune, India) for 60 s. Thin films were deposited on 10 mm × 10 mm Si(100) p-type substrates. Before deposition, the silicon substrates were cleaned with a three step standard RCA cleaning procedure [23] (see Supplementary information for complete procedure). The deposition was done in high vacuum conditions with a base pressure of 10^{-5} mbar and working pressure of 10^{-4} mbar. The substrate to target distance was kept to be 250 mm. Thickness of the film was monitored by using digital quartz crystal thickness monitor (DTM) by inputting the density and acoustic impedance values of Mg:ZrO_2 as 5.68 g/cm^3 and 43.3 × 10^6 dyne s/cm^5 respectively. Electron gun was operated at 5.2 kV by varying current between 120 and 150 mA. Thin films of 0 mol% (pure ZrO_2) and 3 mol% Mg: ZrO_2 each of thicknesses 100 nm and 300 nm were deposited. All these film samples were post-annealed at 500 °C after deposition.

2.2. Fabrication of MOS capacitors

A schematic diagram of a typical fabricated MOS capacitor is shown in Fig. 1a. The top and bottom electrodes used were silver metal deposited by thermal evaporation. The silver electrode layers were deposited up to the thickness of 500 nm with the same vacuum conditions as in the case of electron beam deposition of the oxide layer. The top contacts were deposited with a mask containing 1 mm × 1 mm squares. The top contacts of the MOS devices can be viewed in the photograph shown in Fig. 1b. Each small square is a silver contact acting as a single MOS capacitor. There are sixteen MOS capacitors fabricated on a single piece of 1 cm × 1 cm Si wafer.

2.3. Characterization

Differential scanning calorimetry (DSC) and thermogravimetric analysis (TGA) on the as-prepared powder samples were done at a heating rate of 20 °C per minute (Model: Q600 SD and Q20 DSC, TA instruments). Structural analysis of Mg: ZrO_2 powder was done in a powder x-ray diffractometer (Model: Ultima-IV, Rigaku) by using a Cu-$K_{\alpha 1}$ radiation in the reflection geometry. The XRD patterns for powders were acquired in a 2θ range from 25° to 60° with a step size of 0.02°and the integration time was 1 s in each step whereas for thin films those were acquired in a 2θ range from 25° to 80° with a step size of 0.2° and integration time was 5 s in each step. Crystallite size was calculated by using Debye Scherrer formula from the FWHM of the XRD peaks. Raman spectroscopy was done in a Renishaw In Via system with a laser excitation wavelength of 514 nm. Elemental composition and thickness of the thin films were determined by using Ion beam analysis in which Rutherford backscattering spectrometry (RBS) and Resonant Rutherford backscattering spectroscopy (RRBS) were done. The RBS experiment was carried out with $^4He^+$ ion beam in a HVEE (High Voltage Engineering Europa) made 1.7 MeV tandetron accelerator. The RBS was done by using 2 MeV $^4He^+$ beam and the RRBS was done by using 3.05 MeV incident beam energy for $^{16}O(\alpha,\alpha)^{16}O$ resonance elastic scattering. The backscattered alpha particles were detected by a surface barrier silicon detector (energy resolution of 20 keV) at a scattering angle of 165° from the incident beam direction. The surface topography of the deposited thin films were evaluated by using Atomic Force Microscopy (NTEGRA, NTMDT Russia) in tapping mode operation. The capacitance-voltage (C-V) characteristics of the MOS devices were measured at 1 kHz frequency in the voltage window ranging from − 2 V to + 2 V by using Agilent E14980A LCR meter at 1 V biasing voltage. The current-voltage (I-V) characteristics were measured in the voltage range from 0 to −15 V by using a Kiethley 238 current source meter.

3. Results and discussion

3.1. Thermal analysis

For achieving the desired crystalline thin films in the fabrication process of MOS capacitors crystallization temperature must be known for the dielectric material used. In order to find the crystallization temperature thermal analysis of the as-prepared pure and Mg:ZrO_2 powders was done. Fig. 2 shows DSC thermograms and the corresponding weight loss (%) of the as-prepared ZrO_2. An endothermic peak observed between 30 °C and 200 °C corresponds to a weight loss of 26% due to the dehydration process by loss of water content and other volatile compounds such as precursor chlorides and ammonia [24] those might have remained in the precipitates after washing. An exothermic peak observed at 425 °C corresponding to a weight loss of 3% can be due to crystallization process in the pure ZrO_2 powder. Whereas in case of Mg:ZrO_2 the exothermic peak observed at 475 °C had slightly shifted to higher crystallization temperature. It has been reported that the crystallization temperature is directly proportional to the dopant concentration and inversely proportional to the ionic radius of dopant cation when studied for different undersized dopant ions in ZrO_2 crystal system [25]. This could be the possible reason for the shift towards higher crystallization temperature because the dopant concentration increases as well as the ionic radii of Mg ion (0.72 Å) is smaller than the same of Zr ion (0.78 Å).