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Improving the quality of Al_2O_3/4H-SiC interface for device applications

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ABSTRACT

The present paper focuses on the investigation of Al_2O_3/4H-SiC dielectric interface upon annealing, its consequent structural modifications, and the link to electrical properties. For this purpose, the test structures are prepared by depositing Al_2O_3, using atomic layer deposition (ALD), on low doped n-type 4H-SiC epitaxial layers. The structures are annealed from 300 °C to 1100 °C for different time duration (from 5 to 60 mins) and ambient such as, low vacuum (10^{-1} Torr), N_2, and N_2O. The structural studies on these samples are conducted using synchrotron-based high resolution x-ray photoelectron spectroscopy (HR-XPS), lab-based XPS, time of flight elastic recoil detection analysis (ToF-ERDA), and time of flight medium energy ion scattering (ToF-MEIS). The electrical response of capacitive structures is monitored through capacitance voltage (CV) measurements for as-deposited and annealed structures. It is found that the annealing at high temperatures, such as 1100 °C, and in N_2 or N_2O environment, improves the dielectric properties due to the introduction of a thin layer of about 1 nm stable SiO_2 between the Al_2O_3 and 4H-SiC.

1. Introduction

The development of SiC technology for power electronics' applications is rapidly growing and many different types of devices have been developed, mainly due to the access to high quality material and relatively well understood processing steps [1]. Now, with increasing commercialization, reliability of SiC devices is a major concern [2], where the gate and/or passivation dielectric plays a vital role. Silicon dioxide (SiO_2) has so far nurtured the development of SiC-based power devices, thanks to Si-technology [3]. However, a much lower value of the dielectric constant of SiO_2 (ε_r = 3.9) does not allow exploitation of 4H-SiC (ε_r = 9.7) to its full potential. Moreover, the SiO_2 dielectrics on SiC generally results in low surface mobilities, poor reliability, lower breakdown fields, and lower temperature operation [4]. Thus, a strong motivation to find an alternate dielectric solution to enhance the performance of 4H-SiC based devices exists.

Compared to other high-k dielectrics studied over last few years, Al_2O_3 has appeared a better choice for 4H-SiC [5–13] due to its suitable material properties, for instance, good thermal stability, high band offsets with SiC conduction and valence bands (ΔE_c = 1.84 eV and ΔE_v = 1.9 eV, respectively), wider bandgap (7–8.8 eV), high dielectric constant (7–9 eV), and high breakdown field (E_B = 10–13 MV/cm) [14,15]. Despite promising electrical characteristics, a major problem highlighted in the literature for Al_2O_3/4H-SiC interface is the high concentration of interface states and fixed charges in the oxide. It is also not easy to incorporate Al_2O_3 in device processing due to the unclear behavior of its interface with 4H-SiC under different processing conditions. In particular, surface preparation prior to ALD deposition process, post-deposition annealing, annealing time and ambient have significant effects on the interface and its electrical response in terms of fixed oxide charges and D_{it} [16]. Usually for most of the processes, the growth of thin SiO_2 at the interface is highly likely, which is not at all a drawback, but it helps in improving the performance of MOS-based devices [17] by adding an offset in the dielectric/4H-SiC structure, as can be seen in band diagram shown in Fig. 1. However, a good control of the interfacial oxide can significantly enhance the performance of the device [17]. Therefore, finding a concrete solution to these process related issues, it is of utmost importance to understand the structure and stoichiometry of Al_2O_3/4H-SiC dielectric interfaces, and also the processing parameters affecting the interface, prior to the integration of Al_2O_3 into commercial devices as an alternate dielectric.

The main objective of the present paper is to acquire an atomic-level understanding of chemical bonding at the interface of Al_2O_3/4H-SiC structures in as-deposited and annealed form, and the consequence of annealing on the electrical response of the interface. Here we have summarized the effect of above-mentioned processes on the structural characteristics measured through x-ray photoelectron spectroscopy (XPS), medium energy ion scattering (MEIS), and elastic recoil

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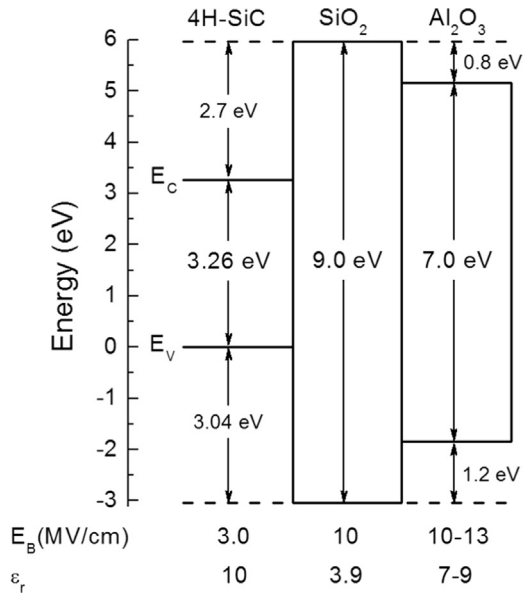

Fig. 1. Band alignment of the Al_2O_3/SiO_2/4H-SiC. The values presented here are for ALD deposited films on 4H-SiC [14,15]. The band offsets are adjusted according to scale.

detection analysis (ERDA). Moreover, the implication of annealing conditions on the electrical response is observed through CV and IV measurements. It is seen that high temperature post dielectric deposition annealing is fruitful in term of reducing oxide charges and improving the IV characteristics for device applications.

2. Fabrication and characterizations

Epitaxial 4° off-axis layers of 4H-SiC with nitrogen doping of ~ 10^{15} cm^{-3} was used in fabricating test structures for the present investigations. A few samples with similar amount of p-type doping were also arranged for comparison [18]. The wafers were diced in 1 × 1 cm^2 small pieces. These samples were cleaned through a standard cleaning process [7 up (3000 ml H_2SO_4: 1000 ml H_2O) + IMEC (6000 ml DI H_2O: 60 ml isopropanol: 60 ml HF (50%))]. A few samples were further cleaned in weak RCA, followed by additional RCA cleaning treatments (see details in refs. [16,19]). After all cleaning treatments, the samples were dipped in HF (5%) to remove the native oxide from the surface of 4H-SiC. Immediately after this, Al_2O_3 was deposited using BENEQ TFS 200 atomic layer deposition system. The deposition was done at 200 °C using trimethylaluminium (TMA) as an Al precursor and deionized (DI) water (H_2O) as oxygen precursors. The Al_2O_3 was deposited in different thicknesses, from 2.5 to 50 nm, by varying the number of ALD cycles. The samples were later treated with post dielectric deposition annealing (PDA) at various temperatures from 300 °C to 1100 °C for different time durations (from 5 to 60 mins). The annealing was performed in low vacuum (10^{-1} Torr), N_2, or N_2O ambient. For electrical measurements, top and bottom contacts were prepared by sputtering of 500 nm Al. Circular top contacts with a diameter of 50–500 μm were then formed.

The high resolution (HR) XPS measurements were performed on 2.5 nm thick Al_2O_3/4H-SiC samples using the synchrotron light source at the Swedish National Synchrotron Radiation facility MAXlab, in Lund, using 250, 400, 650 and 1050 eV photon energies [20]. Additional XPS measurements on 3, 6, and 10 nm thick Al_2O_3 were conducted on a Scienta-Omicron XPS system equipped with a micro-focused monochromatic Al K-Alpha (1486.7 eV) at the National Centre for Physics, Islamabad, Pakistan. In all XPS measurements, Si2p, C1s, Al2p, and O1s core level spectra were collected for all as-deposited and annealed samples. ERDA for as-deposited samples was also conducted using a ^{127}I beam with an energy of 36 MeV and incident and exit angles for the ions relative to the surface normal was 67.5°. ToF-MEIS was

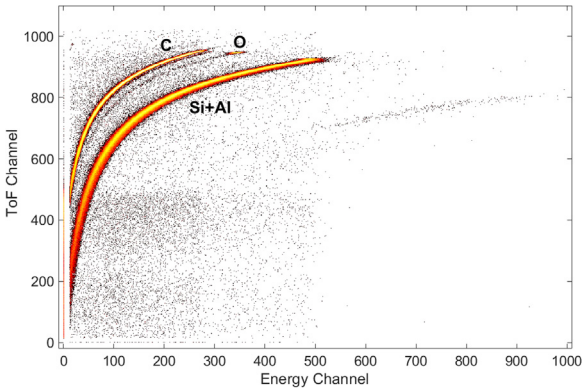

Fig. 2. ToF-ERDA data of as-deposited films 10 nm Al_2O_3 on 4H-SiC.

employed to analyze the Al_2O_3/4H-SiC structures using a 60 keV helium beam with a position sensitive delay line detector at 65° relative to the normal and the backscatter angle was 115° [21]. CV measurements were performed using a Keithley 4200-SCS parameter analyzer, with frequencies ranging from 1 to 200 kHz at room temperature.

3. Results and discussion

Fig. 2 shows ToF-ERDA measurements conducted on as-deposited Al_2O_3 (10 nm)/SiC samples. The results confirmed the stoichiometry and thickness of the deposited films. Additionally, a sharp interface between Al_2O_3 and 4H-SiC in as-deposited form was verified [13,22]. The 900 °C annealed samples (in 10^{-1} Torr vacuum) were also measured and showed slight diffusion of oxygen in to the SiC, which could be due to the formation of an interfacial oxide. In few of these measurements, a minute quantity of Na was found at the surface in annealed samples, which could have been originated from contamination in the annealing furnace.

Fig. 3 presents the HR-XPS results obtained at 650 eV for Si 2p core level spectra of the as-deposited, 700, and 1100 °C annealed Al_2O_3 (2.5 nm)/4H-SiC structures. The annealing was done for 60 min in N_2O. It was clearly observed that the as-deposited films only show Si from the SiC substrate. However, upon annealing at 700 °C, a smaller peak with higher binding energies appears, which depicts the partial oxidation of

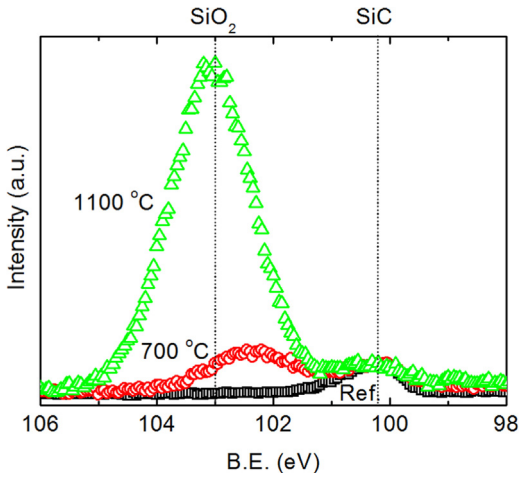

Fig. 3. HR-XPS measured with 650 eV incident photon energy. Si 2p from SiC and formed SiO_2 as a result of annealing for 60 mins can be seen at 100.2 eV and 103 eV respectively. The samples used for these measurements were cleaned with standard cleaning process and annealed in N_2O. The Si 2p peak from SiC is referenced to 100.2 eV [23] to make a good comparison.