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Improved device characteristics obtained in 4H-SiC MOSFET using high-k dielectric stack with ultrathin SiO_2-AlN as interfacial layers

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ABSTRACT

A novel method of stacking dielectric layers on top of Silicon carbide (SiC) is proposed to address the most common Silicon dioxide (SiO_2)-SiC interface issues in SiC based metal oxide semiconductor (MOS) devices. Aluminum nitride (AlN) as an interfacial layer, instead of SiO_2, between hafnium oxide (HfO_2) and SiC showed improved device characteristics. However, incorporating SiO_2 along with AlN as an interfacial layer is found to be the best way of stacking dielectric layers. This is concluded, based on the changes observed in the electrical characteristics of the device by intentionally varying lattice temperature (T), interface trap density (D_{it}) and junction field effect transistor (JFET) width. All the investigations are done in 4H-SiC half-cell planar n-channel MOS field effect transistor (MOSFET) using commercially available technology computer aided design (TCAD) software sentaurus device. Theoretical calculations show good agreement with the simulated results, and are compared with the published results.

1. Introduction

SiC based power MOSFETs are regarded as promising devices for applications which require faster switching and withstand higher temperatures without losing device properties [1,2]. The full potential of SiC devices has not been realized due to low field effect mobility resulting from the high density of traps at the SiO_2-SiC interface [3]. It is challenging to design a device which has high channel mobility, low specific on resistance ($R_{on,sp}$), and high blocking voltage simultaneously as there exists a trade off between these device parameters. The choice of gate insulator plays a crucial role in the performance of the device, especially on the channel mobility. In addition to coulomb scattering due to interface traps, there could be other scattering mechanisms such as impurity scattering, a phonon scattering, and surface roughness affecting the channel mobility [4]. The source of interface traps is primarily due to dangling bonds, carbon clusters or carbon-related defects from high-temperature oxidation and the near interface traps located 1–2 nm in the oxide [5,6]. The gate insulator should ideally minimize interface traps and withstand high electric fields during the forward conduction/ reverse blocking mode with low gate leakage currents. In order to withstand high electric fields, the focus has been shifted to other alternative high-k dielectrics. Although HfO_2 as a high-k dielectric has been explored earlier, direct deposition on SiC poses a problem [7,8]. In addition to the high density of surface traps, it leads to high gate leakage currents due to low conduction band offset of about 0.9 eV [9]. Low band offsets increases the probability of carriers tunneling through the dielectric. This issue has been addressed by inserting a thin layer of SiO_2 between HfO_2 and SiC [7,9]. The same is the case with AlN, which provides a conduction band offset of about 1.7 eV. Although AlN and HfO_2 have been individually investigated as high-k dielectric [10], no study has been done with AlN as an interfacial layer between HfO_2 and SiC. AlN provides good lattice matching and thermal expansion properties with respect to SiC. Nevertheless, in this study SiO_2 is also being used as an interface layer in combination with AlN as it provides the highest conduction band offset of about 2.7 eV among the available dielectrics [11]. While AlN provides good thermo-mechanical matching with SiC [12], direct deposition of AlN on SiC does introduce interface trap charges causing high leakage currents. Interface trap density and temperature have been intentionally varied to observe the magnitude of changes AlN introduces in device characteristics. In this paper, we explored sub threshold swing, mobility and $R_{on,sp}$ characteristics in detail as these are important parameters defining the switching speed of the device. Moreover, sub threshold characteristics can also be used to understand the gate oxide performance. Two-dimensional numerical simulations using sentaurus device from synopsys is utilized in this work to interpret the electrical characteristics of the device.

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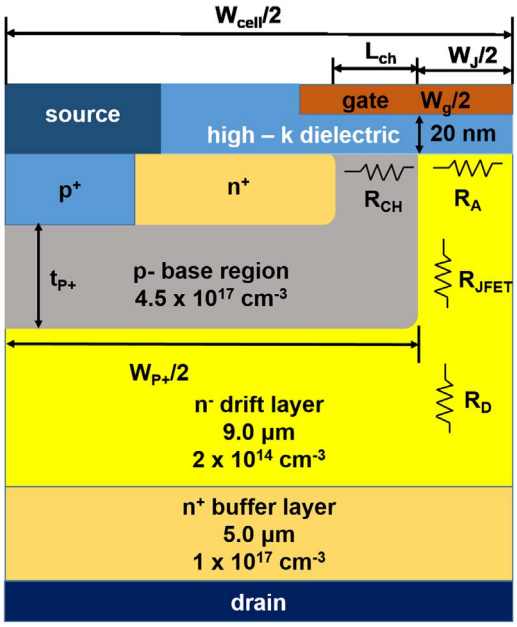

Fig. 1. Schematic view of the half-cell 4H-SiC MOSFET along with doping profile and thickness.

2. Device structure and parameters

A schematic cross sectional two dimensional (2D) view of 4H-SiC half-cell MOSFET along with doping profile and thickness is shown in Fig. 1.

The device structure is made up of p-base region having thickness (t_{P+}) of 2 µm, width ($W_{P+}/2$) of 3 µm, n^+ well having thickness 1 µm, length of the channel (L_{CH}) is of 2 µm, length of the JFET ($W^J/2$) is of 2 µm, length of the gate ($W_g/2$) considered slightly above 4 µm in contact with the source of n^+ region. The device contacts source, drain and gate chosen to be Aluminum metal with a work function of 4.26 eV. Half-cell structure of the device is chosen due to its simplified simulation time and mesh grid count. The device is calibrated with fine meshing in the crucial areas like channel of the MOSFET, MOS interface, JFET region and the junction between p-type and n-type semiconductor regions with the total number of 32,000 mesh points while mesh resolution at the interfaces being 0.3–0.6 nm. Fine meshing enables to extract the results with a greater degree of accuracy. The cell pitch of the device ($W_{cell}/2$) is 5 µm with a width of 1 µm giving an active area of 5 µm × 1 µm. Physics based simulation of the device is carried out by considering band gap narrowing model, Auger recombination model, Shockley-Read-Hall (SRH) recombination, doping-electric field-temperature dependent field mobility models and incomplete ionization model [13]. In addition, all the simulations are carried out taking Fermi-Dirac statistics and multidimensional dependent anisotropic effects (Aniso) into consideration. A full description of the models used can be found in reference [13]. The device structure is constructed based on the reference [14], and the basic I-V characteristics are verified before changes are made to the structure. There are few scattering mechanisms such as phonon scattering, surface roughness scattering, impurity scattering and coulomb scattering that degrade the channel mobility. Lombardi model is considered for mobility degradation in this work. This model has been chosen and verified for SiC MOSFET simulations [15]. Table 1 lists various dielectric properties used in the paper.

Since the dielectric constant of AlN and HfO_2 is higher than SiO_2, the physical thickness of high-k dielectric needs to be increased in order to maintain the same capacitance. The physical thickness of AlN and HfO_2 are shown in Table 1 representing an EOT of 5 nm. Eq. (1) is used for calculating thickness of oxide for a given EOT value.

Table 1
Dielectric parameters used in this work.

Material	SiO_2	AlN	HfO_2
Dielectric constant (ε)	3.9	8.5	22
Bandgap E_g (eV)	9.0	6.23	5.9
Δ E_C (eV) with respect to SiC [11]	2.7	1.7	0.9
Δ E_V (eV) with respect to SiC [11]	3.1	1.3	1.16
EOT (nm)	5	10.9	28

Table 2
Mobility parameters for 4H-SiC.

Parameter	Quantity	Units
mu1n.caug	40	cm^2/V-s
mu2n.caug	950	cm^2/V-s
ncritn.caug	1.94×10^{17}	cm^{-3}
alphan.caug	0.61	arbitrary
mu1p.caug	15.9	cm^2/V-s
mu2p.caug	125	cm^2/V-s
ncritp.caug	1.76×10^{19}	cm^{-3}
alphap.caug	0.34	arbitrary
betan.caug, betap.caug	2	arbitrary
v_{satn}, v_{satp}	2.2×10^{17}	cm^2/s

V = volt, cm = centimeter, s = second.

$$T_{OX} = EOT * \frac{\epsilon_{OX}}{\epsilon_{SiO_2}} \quad (1)$$

The following equation is used for calculating thickness of dielectric stack with SiO_2 as interfacial layer.

$$T_{high-k} = (EOT - SiO_2) * \frac{\epsilon_{high-k}}{\epsilon_{SiO_2}} \quad (2)$$

The mobility parameters used in device simulation are listed in Table 2 and the material parameters in Table 3. Table 2 lists some of the key parameters of temperature, doping and high field dependence mobility models. The insulating material is replaced with multiple dielectrics as follows I) HfO_2 (18 nm)-SiO_2 (2 nm) II) HfO_2 (18 nm)-AlN (2 nm) III) HfO_2 (17 nm)-SiO_2 (1 nm)-AlN (2 nm). The individual thickness values mentioned are fairly approximate values adjusted to EOT of 5 nm with HfO_2-AlN slightly lower than 5 nm. The $R_{on,sp}$ for 4H-SiC MOSFET is given by the summation of Eqs. ((3), (4), (5) and (6)) known for sum of channel resistance (R_{CH}), accumulation resistance ($R_{A,SP}$), JFET resistance ($R_{JFET,SP}$), drift resistance ($R_{D,SP}$) i.e., $R_{on,sp} = R_{CH} + R_{A,SP} + R_{JFET,SP} + R_{D,SP}$ from source to drain. The equations are taken from reference [16], and are used for calculations of

Table 3
Material parameters for 4H-SiC.

Parameter	Quantity	Value
Eg_{300} (eV)	band gap at 300 K	3.24
ϵ	dielectric constant	9.66
ϵ_{Aniso}	dielectric constant - aniso	10.03
A_{UGN} (cm^6/s)	Auger-recombination parameter for electron	5×10^{-31}
A_{UGP} (cm^6/s)	Auger-recombination parameter for hole	2×10^{-31}
N_{srhn}	SRH concentration dependent lifetime model for electron	1×10^{16}
N_{srhp}	SRH concentration dependent lifetime model for hole	1×10^{16}
A_{RICHN} (A/K^2 cm^2)	effective richardson constant for electrons	146
A_{RICHP} (A/K^2 cm^2)	effective richardson constant for holes	30
Gv_b (eV)	degeneracy factor for valence band	4
Gc_b (eV)	degeneracy factor for conduction band	2
LT.TAUN	lifetime model parameter for electrons	4
LT.TAUP	lifetime model parameter for holes	4

1 eV = 1.602×10^{-19} J, eV = electron volt, m = meter, A = ampere, J = joule, K = kelvin, nm = nanometer, cm = centimeter, C = centigrade.