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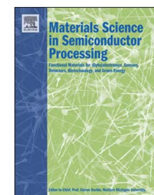

Studies of buried oxide properties on nanoscale GeOI pMOSFETs for design of a high performance common source amplifier

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ABSTRACT

Using well-calibrated TCAD simulation we explore, for the first time, the impact of buried oxide (BOX) thickness and dielectric constant on the analog circuit performance of 30-nm ultra-thin body germanium-on-insulator (GeOI) pMOSFETs. Our findings show that GeOI MOSFETs with a 20 nm SiO_2 BOX offer lower subthreshold leakage current, high transconductance, improved transconductance generation factor and high intrinsic voltage gain. Furthermore, while GeOI MOSFETs with a 20 nm thin HfO_2 BOX exhibit the lowest output conductance and highest voltage gain, GeOI MOSFETs with a 200 nm thick HfO_2 BOX yield the highest transconductance and unity gain cut-off frequency. Moreover, we design common source amplifiers using GeOI pMOSFETs, analyze and optimize their performance. Our results show that the highest amplifier gain of 6.18 and gain bandwidth of 15.32 GHz are obtained with 20 nm HfO_2 BOX while the highest bandwidth of 3.85 GHz is achieved at BOX thickness of 200 nm.

1. Introduction

Recently, Ge channel MOSFETs have received extensive research attention with a view to replacing conventional Si MOS devices, particularly in the sub-22-nm technology nodes because Ge exhibits outstanding electron and hole mobilities, low energy gap, compatibility to matured Si process technology and also low processing temperature as compared to Si [1–6]. The excellent electron and hole mobilities in Ge are attributed to the lower effective mass of both carriers [7]. However, Ge MOS devices suffer from a couple of shortcomings which include poor interface quality between Ge and gate oxides, and its larger dielectric constant compared to Si [8,9]. Notably, ultra-thin body germanium-on-insulator (GeOI) p-MOSFETs have shown improved performance [10–12] owing to their better electrostatic integrity and augmented hole mobility. Recent technological advancement in the growth of high-k gate dielectrics such as HfO_2, ZrO_2, Al_2O_3, etc. and their subsequent processing enable considerable improvements in the Ge/high-k interface properties. For instance, with the adoption of the advanced composite $HfO_2/Al_2O_3/GeO_x/Ge$ gate stacks, the equivalent oxide thickness (*EOT*) was scaled down to 0.7–0.8 nm while maintaining the interface-trapped charge density (D_{it}) at a considerably low level [13]. Since Ge has a higher dielectric constant, Ge MOSFETs facilitate easy charge sharing between the source and the drain thereby exhibiting early onset of short channel effects. There have been some reports regarding control of short channel effects (SCEs) in Ge channel MOSFETs [14,15]. Furthermore, some studies were reported on the analog and mixed-mode circuit performances of GeOI MOSFETs [16]. More recently, the effect of different buried oxides on the surface roughness scattering limited hole mobility in ultrathin GeOI MOSFETs is reported [17]. Careful literature screening reveals that the BOX thickness scaling [18–20] and dielectric constant variation of BOX [21,22] impact the electrical performance in SOI MOSFETs with the reduced amount of SCEs for a thinner BOX layer having a lower value of BOX dielectric constant. The most intriguing aspect is that the influence of BOX in modifying the device parameters becomes different when Si channel is replaced by Ge as outlined below. BOX dielectrics are represented by dint of dielectric constant, thickness, and also the interface-trapped charge densities at the Ge/BOX interface. The dielectric constants of Ge and Si are 16 and 11.7, respectively. Due to much higher value of dielectric constant the field distribution within the Ge channel becomes much stronger compared to Si channel for a given bias condition. In addition the interface between Ge and BOX exhibits a larger amount of interface-trapped charge density, which influences the landscape of field lines in the vicinity of the interface and also the hole mobility. Moreover, the conduction and valence band offsets associated with Ge/high-k dielectric are quite different than the corresponding values for Si channel devices. Taking these effects all together, it turns out that the current-voltage relationship for a Ge pMOSFET is quite

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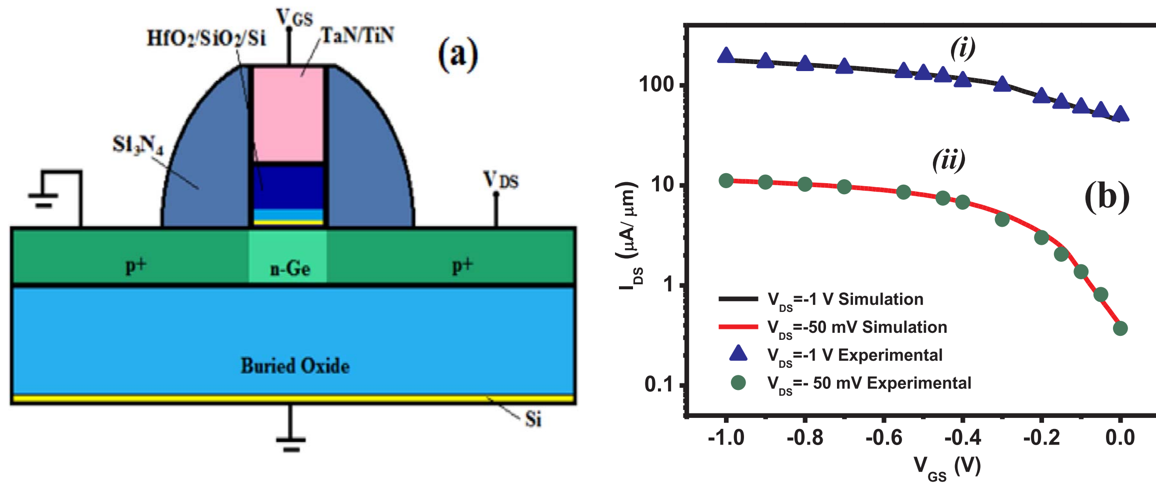

Fig. 1. (a) Schematic diagram of a GeOI pMOSFET and (b) comparison of experimental and simulation transfer characteristics of a GeOI pMOSFET for (i) $V_{DS} = -1$ V and (ii) $V_{DS} = -50$ mV.

different from its Si counterpart for various BOX dielectrics. Therefore a separate exploration on Ge pMOSFETs is needed in order to analyze the impact of BOX on various device parameters of GeOI transistors and also on circuits built using them. While previous investigations of GeOI devices were mostly focused on varying channel thickness, advanced gate dielectrics and reduced source/drain contact resistance for their applications in both analog and digital domains [8,13,16,23], there has been no report of the impact of BOX properties on device parameters related to analog performance and also their subsequent use in analog circuits.

In this paper, we thoroughly examine the impact of buried oxide (BOX) thickness and its dielectric constant on various device parameters of nanoscale UTB GeOI pMOSFETs. Furthermore, we uncover physical insights by analyzing the effect of BOX parameters in modifying the device parameters related to analog circuit applications and also design a common source amplifier together with a detailed analysis for obtaining its optimized performance in terms of gain, bandwidth and gain bandwidth product.

2. Device structure and simulation framework

Fig. 1(a) shows the schematic diagram of a GeOI pMOSFET which consists of composite $HfO_2/SiO_2/Si$ gate dielectric stacks and TaN/TiN gate materials. The thickness and dielectric constant of the constituent gate dielectrics are such that they produce an equivalent oxide thickness (EOT) of 1.6 nm. The front-gate material has a work function of 5 eV. Although the BOX/channel interface-trapped charge density D_{itb} varies in the range 9×10^{11} to 5.9×10^{12} cm^{-2} eV^{-1} for different BOX dielectrics in accordance with the earlier findings [24–28], we fix D_{itb} at 1×10^{12} cm^{-2} eV^{-1} for all BOX insulators to compare various device parameters of GeOI devices related to analog circuit performance with the variation in K_{BOX} and t_{BOX}. The conduction and valence band offsets of various BOX dielectrics with respect to Ge are also included in the simulation. The device design parameters and bias conditions used in the simulation are chosen according to the Radio Frequency and Analog/Mixed-Signal Technologies section of the International Technology Roadmap for Semiconductors (*ITRS*) [29] and are listed in Table 1.

Current voltage characteristics of different GeOI pMOSFETs are obtained using the numerical device simulator, SILVACOATLAS [30]. In the simulation, we use CVT Lombardi mobility model for inversion hole charges in the channel, Hurkx band-to-band tunneling model [31,32] and trap-assisted tunneling model [32,33]. In order to capture the carrier recombination events in the channel we enable Shockley-Read-Hall (SRH) and Auger recombination models. The carrier distribution at

Table 1
Various device design parameters of GeOI pMOSFET.

Device parameters	Value
Channel length	30 nm
Channel thickness	10 nm
Channel width	1 μm
Channel doping concentration	2×10^{17} cm^{-3}
Front gate D_{it} [25]	9×10^{11} cm^{-2} eV^{-1}
Fixed Buried Oxide D_{itb}	1×10^{12} cm^{-2} eV^{-1}
BOX thickness	20, 50, 100, 200 nm
BOX dielectric constant	3.9, 9.3, 12.2, 22
Supply voltage V_{DD}	−1 V

different energies is determined using Fermi-Dirac (FD) distribution function in our analysis. We invoke the drift-diffusion current density model for the transport of carriers in the channel. Furthermore, Newton's method is used in order to obtain accurate solutions to several coupled equations employed in the simulation.

We have calibrated our model by comparing the experimental transfer characteristics of GeOI device having channel thickness of 25 nm and channel length of 30 nm [11] with our simulated transfer characteristics as shown in Fig. 1(b) at both low and high drain to source bias voltages, $V_{DS} = -50$ mV and -1 V. It is evident from Fig. 1(b) that our simulated transfer characteristics show good agreement with the reported experimental transfer characteristics for both high and low values of V_{DS}. This fact ensures the validity of our simulation framework.

3. Results and discussion

We intend to carefully study the impact of BOX thickness and dielectric constant on various device parameters such as transconductance g_m, transconductance generation factor g_m/I_{DS}, output conductance g_d, intrinsic voltage gain A_v and cut-off frequency f_T of GeOI pMOSFETs. The detailed physical insight obtained from device level analysis is employed to design common source amplifiers using GeOI pMOSFETs and optimize their performance with reference to BOX thickness and dielectric constant, and also load resistance.

3.1. Impact of BOX dielectric constant K_{BOX} and thickness t_{BOX}

In the present study we employ four BOX insulators such as SiO_2, Al_2O_3, GeO_2 and HfO_2 having dielectric constant of 3.9, 9.3, 12.2 and 22, and they are represented using rectangular black, circular red, triangular blue and star olive color symbols, respectively in all the Figs. 2

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