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Recent advances in 4H-SiC epitaxy for high-voltage power devices

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ABSTRACT

This paper reports recent advances in high-quality 4H-SiC epitaxial growth. The modern 4H-SiC epitaxial reactors, techniques to improve growth rates and large-diameter uniformity and reduce defect densities are discussed. A single-wafer vertical-type epitaxial reactor is newly developed and employed to grow 150 mm-diameter 4H-SiC epilayers. Using the reactor, high-speed wafer rotation is confirmed effective, both for enhancing growth rates and improving thickness and doping uniformities. Current levels of reducing particle-induced defects, in-grown stacking faults and basal plane dislocations and controlling carrier lifetimes are also reviewed.

1. Introduction

Silicon carbide (SiC) power devices outperform conventional silicon devices in terms of current conduction and switching and are expected, as new-generation technology, to help reducing CO_2 emissions through low-loss power conversion [1,2]. The practical use of 4H-SiC Schottky barrier diodes (SBDs) and metal-oxide-semiconductor field effect transistors (MOSFETs) has started in various applications [2,3]. From the semiconductor industry perspective, the evolution of crystal growth techniques achieving lower material costs and defect densities is desirable to sustain the wide-ranging applications of 4H-SiC power devices.

The standard 4H-SiC wafer production includes growing a SiC bulk crystal, slicing the bulk crystal, polishing wafers and performing epitaxial growth [4]. Chemical vapor deposition (CVD) is currently the only alternative method for producing 4H-SiC epitaxial layers (epilayers) for power devices. High-quality homoepitaxial growth, maintaining the 4H-SiC poly-type, is realized by a "step-flow control" technique in which an off-angle of a few or several degrees from {0001} faces is engaged on the substrate and the stacking sequence on advancing steps is replicated [5]. At present, (0001) Si-face wafers with 4°-off cut toward <11$\bar{2}$0> are mainly employed to fabricate 4H-SiC SBDs and MOSFETs. As the standard CVD epitaxial growth process, H_2, SiH_4 and C_3H_8 have been used as the carrier, Si-source and C-source, respectively [5]. The Cl-based gas system, adding HCl to the standard gas system or using Cl-containing source gas, is also applied alternatively [6–12]. Precise control of the thickness and doping concentration, maintaining their intra-wafer and wafer-to-wafer uniformities, is requested for the epilayer to comply with the device design. Establishing a technique to produce 150 mm-diameter 4H-SiC epilayers with sufficient uniformities and low defect densities is a current issue in the industry. A high growth rate or short cycle time may also be offered to enhance throughput in epilayer production.

Currently available 4H-SiC substrates still contain high densities of threading dislocations and basal plane dislocations (BPDs). According to their Burgers vector, threading dislocations can be classified into threading screw dislocations (TSDs) with a Burgers vector of c or $c+a$ and threading edge dislocations (TEDs) with a Burgers vector of a /3 <11$\bar{2}$0>, while BPDs have a Burgers vector of a /3 <11$\bar{2}$0> [13–15]. Threading dislocations with a Burgers vector of $c+a$ are also referred to as threading mixed dislocations (TMDs). Typical dislocation densities in commercial 4H-SiC substrates can be 10^2–10^3 cm^{-2} for TSDs, 10^3–10^5 cm^{-2} for TEDs and 10^2–10^3 cm^{-2} for BPDs, respectively. These dislocations in a substrate propagate into an epilayer, while some also change their line direction or convert into partials forming a stacking fault (SF) during epitaxial growth [16,17].

There have been numerous studies on the propagation or conversion of dislocations during 4H-SiC epitaxial growth and the influence of dislocations on device performance. Based on the current understanding, threading dislocations can adversely affect device performance, i.e. leakage current or blocking voltage in the reverse bias or charge to breakdown of the MOS structure, when the dislocations form a pit on the epilayer surface and no significant negative influence is recognized if the surface pits around the dislocations are removed [18,19]. This implies that the threading dislocation density in state-of-the-art 4H-SiC wafers is often within an acceptable level for device fabrication [20]. Conversely, the role of BPDs acting as nucleation sites for single Shockley SFs (SSFs) with the (31) stacking sequence has been

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verified and the SSFs expand when minority carriers are injected exceeding a certain level [21–23]. Accordingly, BPDs are requested to be eliminated from the active region if the device is operated with minority carrier injection, otherwise the injection of minority carriers into a region where BPDs are existing is restricted to within a certain level.

Inclusions and SFs also frequently form in 4H-SiC epitaxial growth. Particle-related "downfall defects" and 3C-triangular defects can contain 3C-SiC particles and triangular 3C-inclusions and kill device performance [24,25]. In-grown SFs with a stacking sequence differing from perfect 4H stacking are another type of defects. The (44) SFs, also referred to as 8H faults [26], are found to significantly decline the breakdown voltage of the SBDs [27]. These defects, which detrimentally affect device performance, must be low enough in epitaxial layers to obtain acceptable yield in the device fabrication. For instance, the production of 1 cm^2-area devices may offer a defect density (killer defects) of less than 0.1 cm^{-2}.

Control of carrier lifetimes in 4H-SiC epilayers is also essential to fabricate bipolar devices. The $Z_{1/2}$ center, confirmed as a mono carbon vacancy, creates an accepter level at Ec-0.63 eV and acts as an effective lifetime killer in 4H-SiC epilayers [20,28–30]. Although modifying the growth conditions can reduce the concentration of the $Z_{1/2}$ center to a certain extent [31], the minority carrier lifetimes in an as-grown 4H-SiC epilayer may remain within several microseconds [32]. Carrier lifetimes in 4H-SiC epilayers can be enhanced far beyond 10 μs by C^+-implantation and thermal oxidation techniques [33,34], both of which utilize diffusion of carbon interstitials from the surface region of the epilayer and mutual annihilation of carbon vacancies ($Z_{1/2}$ defects) inside the epilayer and diffused carbon interstitials. Moreover, an intentional increase in the $Z_{1/2}$ center concentration to control carrier lifetimes in the 4H-SiC epilayer has been demonstrated by electron irradiation and high-temperature annealing [35–38]. Since the concentration of the $Z_{1/2}$ center is influenced by ion-implantation, high-temperature annealing, thermal oxidation and reactive ion etching processes, there may be a need to establish a carrier control technique compatible with device processing.

This paper reports recent achievements in 4H-SiC epitaxial growth toward high-voltage power devices [39]. The evolution of techniques to improve throughput and uniformity, reduce detrimental extended defects and control carrier lifetimes in epitaxial growth process are also reviewed.

2. Modern 4H-SiC epitaxial growth reactor

A hot- or warm-wall configuration is adapted in modern 4H-SiC epitaxial growth for efficient heating of wafers and CVD gases and to reduce the temperature difference between the wafer and susceptor [5,39–41]. Schematic drawings of horizontal hot-wall and planetary warm-wall reactors are shown in Fig. 1A and B. Both types of reactors with a capacity of multiple 150-mm-diameter wafers have been developed. The CVD gases flow horizontally above a wafer in the reactors. Although a thermo-dynamic computer simulation for a horizontal reactor indicates that partial pressures of the gas-species formed in the hot zone vary along the gas-flow direction [42], susceptor or wafer rotation as well as control of gas-flow and temperature distribution in the hot zone significantly improves thickness and doping uniformities for a large-diameter epitaxial layer. Recent results when using horizontal hot-wall or planetary warm-wall reactors show thickness uniformity of ~ 1–2% and doping uniformity of ~ 4–6% in σ/mean values for 150 mm-diameter epilayers [43–45]. Typical growth rates in the reactors can be 5–30 μm/h.

A newly developed vertical 4H-SiC epitaxial reactor is illustrated in Fig. 1C [46,47]. A single 150 mm-diameter wafer is placed on a susceptor, which is then rotated up to 1000 rpm by a mechanical motor. The wafer and susceptor are heated by current-controlled lower and upper resistive heaters, while typical growth (wafer) temperature is 1600–1650 °C. The lower heater placed underneath the susceptor

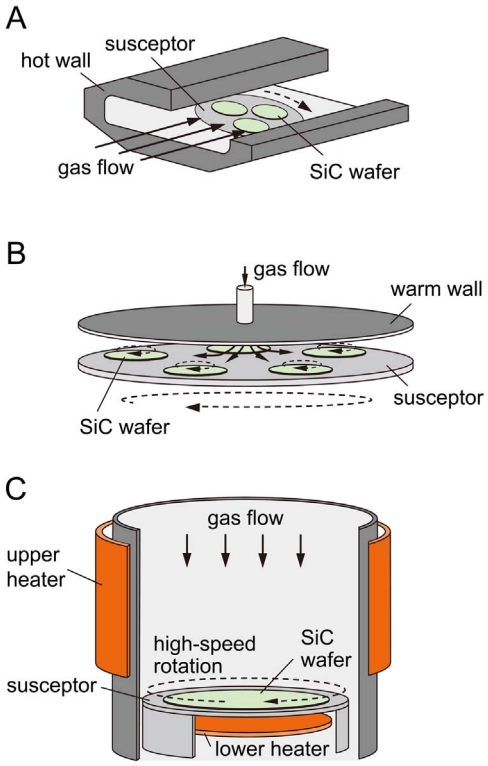

Fig. 1. Schematic illustration of (A) horizontal hot-wall, (B) planetary warm-wall and (C) vertical 4H-SiC epitaxial reactors.

comprises disc-shaped inner and concentric outer heaters. The upper heater is divided into three zones and placed outside a cylindrical wall. The multi-zone heaters precisely adjust the radial distribution of wafer temperature to within ± 2 °C when growing a 150 mm-diameter epilayer. The heating system can also achieve both temperature elevation and cooling between wafer-loading and growth temperatures within 15 min in total and process time of 30 min or less for producing a 10 μm-thick epilayer, given a growth rate of ~ 50 μm/h. Improvements in the growth rate, uniformity and defect density using the reactor are discussed in later sections. We note that a cold-wall vertical epitaxial reactor with high-speed wafer rotation has demonstrated remarkable potential for SiC epitaxial growth in 1990s [48].

3. Enhancement of growth rate

Epitaxial growth of 4H-SiC is practically undertaken in a mass-transport controlled regime. Fig. 2 shows a schematic drawing of the gas-flow and mass-transport in a vertical reactor. When using a H_2-SiH_4-C_3H_8 gas system, gaseous Si, SiH, SiH_2, CH_4, C_2H_2 and C_2H_4 are produced as major gas species by thermal decomposition and contribute to growth [42,49]. Such gas species are supplied to the wafer surface by diffusion through the stagnant boundary layer. The relation between

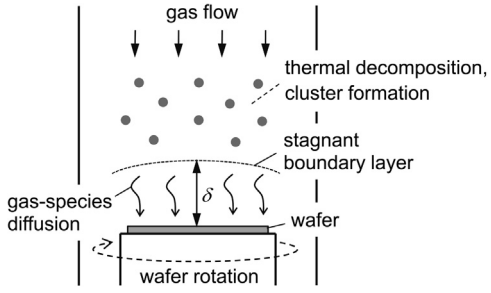

Fig. 2. Schematic drawing of gas-flow and mass-transport in a vertical epitaxial reactor.