Materials Science in Semiconductor Processing xxx (xxxx) xxx–xxx

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Advanced processing for mobility improvement in 4H-SiC MOSFETs: A review

Maria Cabello*, Victor Soler, Gemma Rius, Josep Montserrat, José Rebollo, Philippe Godignon

Centro Nacional de Microelectrónica (CNM-CSIC) Campus UAB, 08193 Cerdanyola, Barcelona, Spain

ARTICLE INFO

Keywords:
Silicon carbide
SiC MOSFETs
Field effect mobility
Interface traps
Power devices

ABSTRACT

This paper reviews advanced gate dielectric processes for SiC MOSFETs. The poor quality of the SiO_2/SiC interface severely limits the value of the channel field-effect mobility, especially in 4H-SiC MOSFETs. Several strategies have been addressed to overcome this issue. Nitridation methods are effective in increasing the channel mobility and have been adopted by manufacturers for the first generations of commercial power devices. Gate oxide doping techniques have also been successfully implemented to further increase the channel mobility, although device stability is compromised. The use of high-k dielectrics is also analyzed, together with the impact of different crystal orientations on the channel mobility. Finally, the performance of SiC MOSFETs in harsh environments is also reviewed with special emphasis on high temperature operation.

1. Introduction

It is today widely recognized that new generations of power devices based on Wide Band Gap (WBG) semiconductor materials with superior material properties for power operation are required for a higher efficiency of power converters, as profusely covered in this special issue. Their critical field is more than one order of magnitude higher than Si, which allows using a thinner and higher conductive epitaxial layer. Consequently, the on-state current losses are drastically reduced. Within the WBG family, SiC is one of the most promising semiconductor materials for power devices fabrication, and indeed several commercial devices are already offered on high volume production.

Specifically, MOSFET device is a key element in modern microelectronics, with applications spanning from highly integrated CMOS to high power devices. As a device, it has really boosted the development of all kind of microelectronic technologies since the 1970's. In power electronics, a technology initially based on Si bipolar devices (BJTs and thyristors), MOSFETs and MOS gate-controlled devices (mainly IGBTs), completely monopolize today's market. Therefore, it seemed logical to endeavor a new generation of SiC power devices based on the development of MOSFET architecture. Indeed, since its demonstration in 1993 [1], SiC MOSFET has been the focus of numerous investigations.

However, the development of low resistance SiC power MOSFETs has been slower than other SiC power switches, like JFETs or BJTs, due to its very low inversion channel mobility values and threshold voltage (V_{th}) high instability. These limitations are mainly caused by a poor quality of the MOS interface, which is affected by large oxide charges and interface trap density (D_{it}) values. However, improvements in the MOS interface quality allowed the realization of commercial SiC MOSFETs operative up to 1.2 kV–1.7 kV, yet, SiC high voltage capability is not fully exploited. The current roadmap for SiC semiconductor industry tentatively predicts the introduction of 3.3 kV–6.5 kV SiC devices in the market in the medium term to compete with their Si-based counterparts.

This review compiles several technological solutions focused to improve the SiC MOS interface toward a main target, to increase the channel carrier mobility. Indeed, regarding mobility in the MOSFET channel, we have to consider two ranges of operation, one at relatively low electric field, just above the V_{th} (typically 5 V), and a second regime at higher field, for MOS gate voltages of 15–25 V. The latter is especially relevant for power electronics converters as it corresponds to the gate operation voltage of the devices. There are several ways to extract the channel mobility, coming from Si technology: a) effective channel mobility (μ_{eff}) is extracted from output curves (dI_{DS}/dV_{DS}), b) field effect mobility (μ_{fe}) is extracted from transfer curves (dI_{DS}/dV_{GS}) and c) hall mobility (μ_{hall}) is extracted under magnetic field using Hall laws. However, in SiC, the electrons generated in the inversion layer are trapped by the high density of interface traps and near interface oxide charges, and it strongly affects the extraction of an accurate mobility value [2]. Accordingly, the concept of apparent channel mobility would better reflect the mobility extracted from the measurements. In the literature, most of the reported mobility values for SiC MOSFET test structures are specifically field effect mobilities. Experimentally, the μ_{fe} versus gate voltage (or electric field) curve typically shows a peak

* Correspondence to: CNM-CSIC, C/ dels Tillers, Campus UAB, 08193 Cerdanyola del Valles, Barcelona, Spain.
E-mail address: maria.cabello@imb-cnm.csic.es (M. Cabello).

http://dx.doi.org/10.1016/j.mssp.2017.10.030
Received 1 August 2017; Received in revised form 18 October 2017; Accepted 20 October 2017

Table 1
Properties of SiC polytypes as compared to Si.

Material	E_g (eV) @300k	μ_n ($cm^2/V\cdot s$)	μ_p ($cm^2/V\,s$)	μ_{fe}* ($cm^2/V\,s$)	Ratio μ_n/μ_{fe}	E_c (MV/cm)	ε_r
Si	1.11	1350	450	500	2.7	0.3	11.8
3C-SiC	2.3	750	40	150	5	1.6	9.6
6H-SiC	3.05	415	90	45	9.2	2.6	9.7
4H-SiC	3.2	950	120	7	135	2.5	9.7
15R-SiC	2.98	600	–	60	10	2.5	9.7

* Average value for either dry or wet oxidation [5].

maximum just after the V_{th} is reached. Then, μ_{fe} decreases upon increasing gate voltage (increasing vertical electric field), as it will be carefully discussed latter in this paper. Eventually, the μ_{fe} peak value can be much higher than the μ_{fe} values at high fields. When considering a possible technological solution for MOSFET improvement, this behaviour must be also taken into account. While in Si technology the μ_{eff} is usually a factor 2.5 lower than the bulk mobility, in SiC, this difference is larger and it depends on the crystallographic structure, i.e. SiC polytype (see Table 1).

It is understood that the decrease of the channel carrier mobility is mainly caused by structural imperfections of the dielectric layer as well as in the interface. All the root causes for traps formation are not known today, but interstitial carbon clusters, Si and C vacancies in the SiC surface, oxygen vacancies in the oxide, and most probably a high strain of interface atomic layers are responsible for the creation of electrically active traps. The presence of electrically active charges in the oxide bulk or at the interface strongly influences the flow of the charge carriers in the conduction channel. The different types of charges [3] and their arrangement are schematically represented in Fig. 1. A modelling of channel mobility as a function of the applied gate voltage is reported in [4] for several types of physical scattering effects. Their relevant results include that D_{it} and fixed charges (Q_{ox}) strongly impact the μ_{fe} peak value at low fields, while surface roughness and Near Interface Oxide Traps (NIOTs) are the main parameters affecting μ_{fe} at high fields. However, if the interface traps are reduced, below 4×10^{11} $cm^{-2}eV^{-1}$, the phonon scattering is a μ_{fe} major limiting effect at low fields. The mobile charges and NIOTs are mainly responsible for the V_{th} instability.

This review is structured as follows. We will first recap some results obtained on the different SiC polytypes. Then, the rest of the paper will be focused on 4H-SiC. We will review the various solutions proposed to increase the poor mobility obtained by standard oxidation (wet/dry) of Si face < 0001 > 4H-SiC. Particularly, we will start presenting nitridation treatments, as well as phosphorus, boron and alkaline earth element doping. Other crystallographic orientation of 4H-SiC will then be considered. Finally, we will apply our knowledge on SiC MOS interfaces to discuss device operation in harsh environment, such as performance at high temperature and radiation hardness.

The review is focused on the n-channel mobility improvement. It is important, when comparing results in different papers of the literature to take into account that reported mobility and D_{it} values strongly depend on method and on the test structure used for parameter extraction. Extracted μ_{fe} decreases when the channel length decreases, when the p-type doping is done by implantation instead of epilayer, and when the surface doping is increased.

2. MOS interface for different SiC polytypes

Among the more than 200 possibilities of SiC crystallographic structures, the so-called polytypes, the most commonly used for device fabrication have traditionally been the 3 C (cubic), 6 H and 4 H (hexagonal) polytypes. Table 1 summarizes main fundamental properties of each polytype, together with Si characteristics for reference. Yet, in most present applications, devices are produced on 4H-SiC polytype, due to its superior and more isotropic bulk carrier mobility. Although most of the results reviewed in this paper concern 4H-SiC, it is also interesting to collect the insights on 3C-SiC and 6H-SiC MOSFETs properties reported in literature.

3C-SiC. If compared to 4H-SiC and 6H-SiC based MOSFETs, the few examples of 3C-SiC MOSFETs reported in the literature systematically exhibit higher μ_{fe} values. This behaviour is corroborated by lower D_{it} (7×10^{10} $cm^{-2}eV^{-1}$at 0.2 eV from electric field (E_C)) and active NIOTs values obtained from their experimental measurements. The fact is that as the 3C-SiC bandgap is smaller than the hexagonal polytypes, the NIOTs that trap electrons from the channel, causing the μ_{fe} degradation, are located within the conduction band, but they do not affect electrons trapping [6].

Different from the rest of SiC polytypes, the lower active D_{it} values obtained in 3C-SiC have allowed the integration of MOSFETs with μ_{fe} values between 75 and 260 cm^2/Vs using a standard dry oxide gate process [7], i.e. without extra nitridation or specific Post Oxidation Annealing (POA) treatment. Accordingly, from the point of view of channel efficiency, 3C-SiC would be the ideal polytype for the fabrication of SiC-based power MOSFET. However, the 3C-SiC polytype has important limitations. Drawbacks include its lower critical field strength or lower thermal conductivity, which limit its application to MOSFET high voltage applications. Moreover, the main issue concerning the use of 3C-SiC is the starting material fabrication and quality. Since 3C–SiC polytype is a metastable crystal phase, it cannot be grown in large wafer size by the sublimation method. Despite original growth methods have been proposed by Hoya, like Chemical Vapor Deposition (CVD) on Si [6,7] or Switch Back Epitaxy (SBE) method, a large density of defects and especially Si-terminated stacking faults (SF) are still present in the available material, which limits 3C-SiC

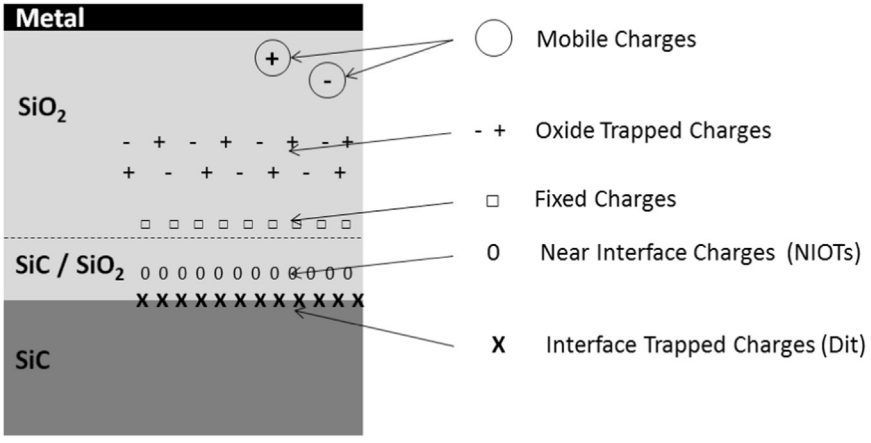

Fig. 1. Schematic representation of the charges present in the SiC MOS interface.