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SiC MOSFET threshold-stability issues

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ABSTRACT

This work provides additional insight into the threshold-voltage instability effect generally observed, to varying degrees, in SiC MOSFETs, and discusses the need for an improved test method to unambiguously separate out good devices from bad ones. Threshold-voltage stability is affected primarily by active charge traps in the near-interfacial region of the insulating gate oxide. Their close proximity to the semiconductor interface leads to a strong time dependence of the direct-tunneling mechanism in response to changes in gate bias. Bias-temperature stressing can induce additional active oxide traps that can then participate in this instability. This time dependence is not properly accounted for in the existing test methods for assessing high-temperature gate-bias (HTGB) effects.

1. Introduction

Potential reliability issues for SiC MOSFETs (metal-oxide-semiconductor field-effect transistors) include threshold-voltage stability [1], gate-oxide reliability [2], body-diode robustness [3], short-circuit current robustness [4,5], and various radiation effects [6–8]. This paper focuses on one of those main potential reliability issues for SiC power MOSFETs—threshold-voltage stability, including a discussion of the main mechanisms involved—but this is not a review paper. Instead, it summarizes recent efforts at the U.S. Army Research Laboratory (ARL) in understanding the potential failure mechanisms associated with threshold-voltage (V_T) drift [9,10], and our efforts to develop an improved test method for separating out good devices from bad with regard to V_T stability [11]. ARL's first paper describing this shift, or drift, in the V_T during gate-bias stressing was published over ten years ago [12], with many other research groups around the world subsequently reporting similar behavior [13–28]. Significant improvements in device processing in recent years have led to much, much smaller V_T shifts by major commercial SiC MOSFET manufacturers [29,30]. Although the main manufacturers of these devices have generally addressed and resolved this issue, the same cannot be said for all new entries into this market. Therefore, it is useful to review the main mechanisms associated with this potential reliability issue, illustrated by either new or previously unpublished results.

If V_T shifts in the positive direction, thus increasing V_T, and if the shifts are large enough, then they may potentially increase the on-state resistance. Similarly, if V_T shifts in the negative direction far enough, then a significant increase in leakage current may occur in the off- or blocking-state. If this increase is large enough, then it may lead to device failure [9].

2. Threshold-voltage instability mechanisms

There are two dominant mechanisms that we have observed, affecting the stability of the threshold voltage: (1) oxide-trap charging and (2) oxide-trap activation. Some appreciable oxide-trap activation must take place during device processing, given that some V_T instability can be readily observed just by gate-bias stressing at room temperature for short durations—although for leading commercial device manufacturers, these shifts are rather small when measured using a standard parameter analyzer, and instead require quite fast measurements of the I_D-V_{GS} characteristics to observe to any appreciable V_T shifts [30]. Older-vintage devices have shown evidence of significant activation during bias temperature stressing, although state-of-the-art devices appear to resist such activation mechanisms [29]. But whatever oxide traps are active, they can and will participate in the oxide-trap charging process when exposed to changes in the applied gate bias.

A typical recent example of the hysteresis observed in the I_D-V_{GS} characteristics, due to this oxide-trap charging effect, is shown in Fig. 1. This fast *I-V* (3-μs sweep time) data was taken using a Keithley 4200-SCS Parameter Analyzer with 4200-BTI-A Ultra-Fast PMU. Because of the very fast sweep employed, less than two full decades of current of are captured—barely in the subthreshold region of this 1200-V, 10-A commercial power MOSFET (a 2015 vintage Vendor A device, consistent with the designations used in [29]), and therefore the current is plotted on a linear scale. This commercially-available device was biased

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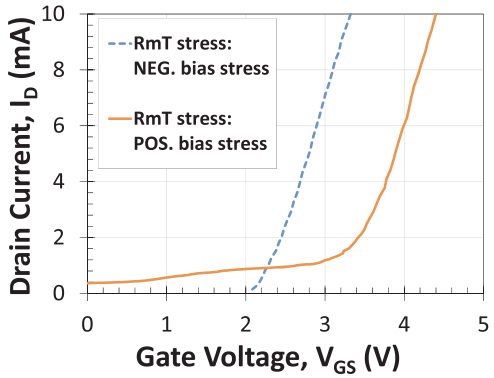

Fig. 1. Variation of the I_D-V_{GS} characteristics (using a 3-μs sweep time) of a commercially-available SiC MOSFET due to alternating positive and negative gate-bias stressing (back-and-forth bias stress)—in this case at room temperature for about 50 μs under each bias condition. V_T was calculated by finding the change in voltage for a constant current.

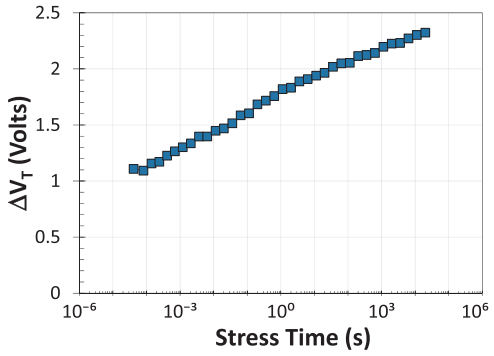

Fig. 2. Variation of V_T hysteresis with stress time of a commercially-available SiC MOSFET exhibits a linear-with-log-stress-time response of V_T instability due to a back-and-forth gate-bias stress sequence. Similar linear-with-log-time responses are observed for unipolar stresses as well, but are smaller in magnitude. The large observed V_T instability is due to the fast *I-V* measurement system employed (using a 3-μs sweep time).

alternately under both positive (+ 25 V) and negative (− 10 V) bias. The hysteresis shown in Fig. 1 is due to a 50-μs bias stress under each bias polarity. The variation in the magnitude of this back-and-forth, or bi-polar stress as a function of stress time under each bias polarity is shown in Fig. 2, ranging from 50 μs to about 2×10^4 s. A linear-with-log-stress-time increase in the V_T hysteresis is what is typically observed, due to the direct tunneling mechanism involved in the charging of the near-interfacial oxide traps [1]. It is instructive that this is a much larger V_T instability than what is observed during a unipolar stress [30].

2.1. Oxide-trap charging

At room temperature, and for short bias-stress times at temperature, the main mechanism causing a shift in V_T is the charging of near-interfacial oxide traps via a direct tunneling mechanism [1,9]. These near-interfacial oxide traps are already present to some degree in as-processed devices, with the specific defect density dependent on the device processing details.

As discussed in more detail elsewhere [31], the rate of change of the charge state of these oxide traps with respect to time is always sharply peaked spatially, with this peak moving into the oxide from the semiconductor interface at a linear-with-log-time rate, giving rise to the notion of a tunneling front (see Fig. 3(a) and (b), for electrons tunneling in and out, respectively). This sharply-peaked tunneling front is a consequence of an exponential decay in the tunneling probability with distance into the oxide, coupled with a sharp transition in the density of available oxide-trap states. Under negative gate bias stress, electrons tunnel out of the oxide (holes tunnel in), uncovering the positively-charged oxide traps (see Fig. 3(c)), causing a negative shift in V_T. Under positive bias, the electrons can tunnel back in, neutralizing this positive charge, and causing a positive shift in V_T (see Fig. 3(d)). This process is generally repeatable *ad infinitum* [9]. This movement of the tunneling front into the oxide at a linear-with-log-time rate also explains, why (for a more-or-less uniform oxide-trap distribution) the V_T instability is generally observed to increase linearly with the log of the stress time, as seen in Fig. 2. Keen observers will notice that Figures (c) and (d) both indicate that both positively-charged and neutralized oxide-trap states always exist right at the interface. This is a consequence of the two-way tunneling model [31], to be discussed in more detail below, which considers the possibility of both electrons and holes simultaneously tunneling into the oxide at any given moment, depending on the availability of an appropriately-charged trap state in the oxide. Thus traps located in the first one or two monolayers of the oxide are constantly changing charge state back and forth.

It is also commonly observed that the magnitude of this V_T instability also increases with increasing applied gate-bias stress, since the tunneling is sensitive to the local field in the gate oxide [1,31]. Furthermore, it is also typically observed that the shift in V_T is more sensitive to the magnitude of the applied gate bias during positive bias stressing, whereas the effect quickly saturates with increasing magnitude of the applied gate bias during negative bias stressing. This effect is well illustrated in Fig. 4, which shows the results of room-temperature gate-bias stressing of older-vintage research-grade lateral MOSFET devices, which had a 500-Å thick thermally grown gate oxide, followed by a standard NO post-oxidation anneal (POA) at 1175 °C. In this case, the measurements were performed with an older, slower Agilent 4145 which had sweep rates approaching 10 s. These results are also consistent with the two-way tunneling model [31], which calculated a strong sensitivity around zero gate bias, such that small changes in low-field conditions could result in relatively large changes in oxide-trap occupation, and thus changes in V_T. This result also suggests that back-and-forth gate-bias stressing, even for small applied electric fields (± 5 V in this example translates to an oxide field of ± 1 MV/cm) will result in a relatively large initial change in V_T. This is certainly the case for the example given in Fig. 2, although the fast *I-V* measurement technique amplifies this effect.

As discussed in great detail elsewhere [9], the stress time determines which oxide traps may change charge state during the bias stress. The longer the stress, the deeper the tunneling front will reach into the gate oxide, resulting in larger V_T instabilities. But given the limits of stress time, some traps will still be too deep to ever change charge state. Although all the oxide traps within reach of this tunneling front may change charge state during the stress, the subsequent measurement time will determine what is ultimately observed. Oxide traps very close to the interface may change charge state during both the stress and the measurement. Thus, only those oxide traps within a certain range of the oxide-semiconductor interface will both switch charge state during the stress and be observed by the measurement. Therefore, faster measurement speeds are needed to measure a greater fraction of the oxide traps that are in fact changing charge state during the stress. This measurement-speed dependence is illustrated in Fig. 5, which shows the results of a two-way tunneling model [31] calculation as a function of measurement speed. More background regarding how these results were calculated, along with agreement with experimental data, are given elsewhere [31].

Fig. 5(a) shows all the oxide traps that will *change* charge state during a 10^5-s negative gate-bias stress which followed a previous 10^5-s positive gate-bias stress (simulating the effects of a back-and-forth stress, as discussed in reference to Figs. 1 and 2), so that the filled in area indicates those oxide traps that changed charge state from neutralized to positively charged due to electrons tunneling out under negative gate bias. As mentioned above when discussing the charge state of traps very close to the interface in reference to Fig. 3, the oxide traps very close to the interface are not likely to ever be fully uncovered