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Current status and perspectives of ultrahigh-voltage SiC power devices

T. Kimoto[a,*], Y. Yonezawa[b]

[a] Department of Electronic Science & Engineering, Kyoto University, A1 Katsura, Nishikyo, Kyoto 615-8510, Japan
[b] Advanced Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba West, 16-1 Onogawa, Tsukuba, Ibaraki 305-8569, Japan

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ABSTRACT

Recent progress in the SiC material and ultrahigh-voltage devices is reviewed. Regarding the material issues, fast epitaxial growth of high-purity epitaxial layers and reduction of basal plane dislocations have made significant strides. Growth technology of 100 μm-thick epitaxial layers intentionally doped to 1×10^{14} cm^{-3} with a basal plane dislocation density of 0.1 cm^{-2} has been established. The carrier lifetimes can remarkably be enhanced by several techniques and trials of lifetime control have been successful. Using very thick (> 100 μm) and high-purity epitaxial layers, 15–27 kV SiC pin diodes and various switching devices such as insulated gate bipolar transistors, thyristors, bipolar junction transistors, and metal-oxide-semiconductor field effect transistors have been demonstrated. Although the performance of these ultrahigh-voltage devices is promising, further improvement of the performance and reliability is mandatory for system applications. Technological challenges in both the material and device fabrication are discussed.

1. Introduction

Owing to recent progress in growth and device technologies of wide bandgap semiconductors, these materials are now realistic candidates for advanced power devices that outperform Si-based devices. Among the wide bandgap semiconductors, silicon carbide (SiC) is especially attractive for high-voltage and high-current applications because of the availability of large-diameter wafers, which enables fabrication of vertical power devices with a large chip size. Other advantages of SiC include p- and n-type doping control in a wide range by either in-situ doping during growth or ion implantation, availability of a native oxide, relatively long carrier lifetimes due to its indirect band structure [1,2]. Since the first production of SiC Schottky barrier diodes in 2001 [3] and that of SiC power MOSFETs in 2010 [4,5], the market of SiC unipolar power devices (mainly 1 kV class) has gradually been growing, demonstrating remarkable energy efficiency in real electronic systems.

In professional power electronics, there exist a variety of applications where very high voltage above 5 kV is handled. Table 1 shows typical examples of such very high-voltage systems. The voltage of distributed power lines is 6.6 kV in Japan and 7.2 kV in USA, where an ultrahigh-voltage blocking capability of 13–15 kV is required for power devices (if constructed without series connection of multiple devices) [6]. The voltage of the main power line for a bullet train (“Shinkansen”) is 25 kV. Furthermore, we see a growing market of high-voltage particle accelerators for medical applications, where the voltage of power supply reaches 10–30 kV. One extreme is high-voltage direct current (HVDC) power transmission, where the voltage usually exceeds 100 kV.

Although the drift resistance of SiC unipolar devices can be much lower than that of Si unipolar devices at a given blocking voltage [1,2,7], the drift resistance significantly increases with increasing the blocking voltage, making very high-voltage unipolar devices less attractive. Fig. 1 plots the ideal forward characteristics of SiC Schottky barrier diodes with several different blocking voltages from 1 to 15 kV and 15 kV pin diodes. In this simulation, a barrier height of 1.2 eV was assumed for the Schottky barrier diodes and the carrier lifetime in the i-layer of the pin diode was assumed to be 10 μs. The limitation of current-handling capability for very high-voltage Schottky barrier diodes is obvious, especially above 10 kV-class blocking voltage. In contrast, the 15 kV SiC pin diode exhibits a very low differential on-resistance owing to the conductivity modulation effect [8]. Though the high built-in potential of a SiC pn junction due to its wide bandgap results in a relatively high turn-on voltage of about 2.8 V, a much higher current density can be achieved in the 15 kV bipolar diode than in the 15 kV Schottky barrier diode at a given power dissipation density (e.g. 300–500 W/cm^2). Since the SiC material is more expensive than Si, it is important to achieve a high current density for reducing the chip size. In real applications, switching loss of power devices must also be considered. In general, bipolar devices exhibit much larger switching loss (reverse recovery for diodes and tail current for insulated-gate bipolar transistors (IGBTs)) than unipolar devices. Cooper and co-workers

* Corresponding author.
E-mail address: kimoto@kuee.kyoto-u.ac.jp (T. Kimoto).

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Table 1
Potential applications of ultrahigh-voltage power devices.

Applications	Voltage
Solid state transformers, loop controllers (distributed power line)	6.6–7.2 kV
Static var compensation (SVC)	7–33 kV
Bullet trains ("Shinkansen")	25 kV
Power supplies for particle accelerators	10–200 kV
High-voltage DC (HVDC) transmission	100–250 kV

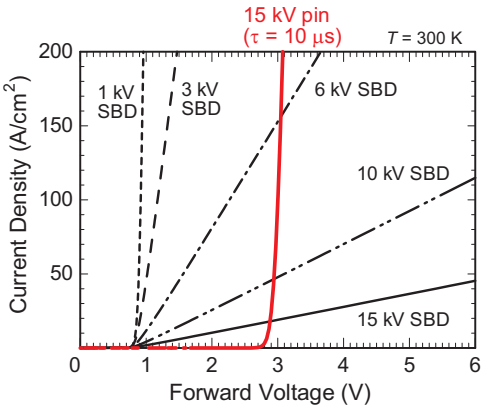

Fig. 1. Ideal forward characteristics of SiC Schottky barrier diodes with several different blocking voltages from 1 to 15 kV and 15 kV pin diodes at room temperature. In this simulation, a barrier height of 1.2 eV was assumed for the Schottky barrier diodes and the carrier lifetime in the i-layer of the pin diode was assumed to be 10 μs.

reported systematic comparison between ultrahigh-voltage SiC bipolar and unipolar devices by using device simulation and suggested the boundary operation conditions where SiC bipolar devices yield lower power dissipation (higher efficiency) [9,10].

Thus, SiC bipolar devices are attractive for ultrahigh-voltage (> 10 kV) applications. In the last decades, various ultrahigh-voltage SiC diodes and switching devices have been demonstrated. However, there exist lots of technical challenges in both the growth and device technologies to fabricate high-performance SiC bipolar devices having sufficient reliability. In this paper, the present status and future challenges associated with ultrahigh-voltage SiC bipolar devices are reviewed.

2. Material requirements

2.1. Doping and thickness

The material requirements to fabricate ultrahigh-voltage (> 10 kV) SiC devices are much different from those for medium-voltage (1–3 kV) SiC unipolar devices. Fig. 2 shows the breakdown voltage vs. the doping density for different thicknesses calculated by using the latest impact ionization coefficients [11]. Very thick SiC with a low doping density below 1×10^{15} cm^{-3} is required for a voltage-blocking layer of 10 kV devices. In the figure, the breakdown voltage increases with decreasing the doping density and saturates at a certain value determined by the thickness. This is a "punch-through limit", where the doping density is low enough for the voltage-blocking region to be completely depleted at a low reverse voltage. In this structure, the electric field distribution is nearly uniform inside the voltage-blocking region, and thereby the required thickness becomes a minimum value for a given blocking voltage. This is actually the optimized design (minimum thickness and sufficiently low doping density) for the voltage-blocking region, because the differential on-resistance is a function of the thickness and not of the doping density in bipolar devices [1,2,8]. Thus the basic design is different from unipolar devices, where the drift resistance is uniquely determined by both the thickness and doping density. For example, an

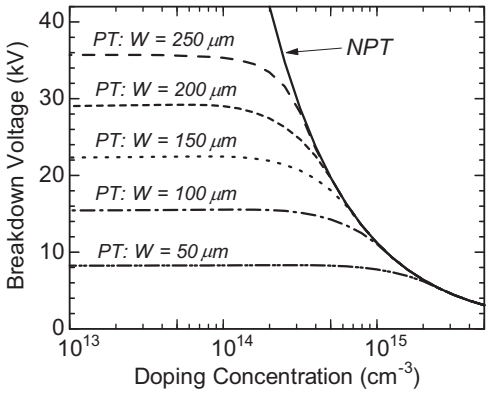

Fig. 2. Breakdown voltage vs. the doping density for different thicknesses calculated by using impact ionization coefficients in SiC. (PT: punch-through structure, NPT: nonpunch-through structure, *W*: thickness of a voltage-blocking layer).

optimum design (doping density, thickness) of the voltage-blocking region is (1×10^{14} cm^{-3}, 95 μm) for 15 kV SiC bipolar devices and (5×10^{14} cm^{-3}, 120 μm) for 15 kV unipolar devices.

Epitaxial growth technology of SiC has made remarkable strides in the last decade. Several groups reported that a lightly-doped epitaxial layer with a net donor density of 1×10^{14} cm^{-3} can be grown by intentional nitrogen doping [12,13]. Note that the doping control in the 10^{14} cm^{-3} range is much easier on SiC(0001) (Si face) than on SiC(000-1) (C face), due to the high nitrogen incorporation on the C face [14,15]. In the state-of-the-art technology, the typical growth rate used for mass production of SiC devices is about 5–12 μm/h. The major challenge in fast epitaxy of SiC is suppression of homogeneous nucleation of Si species (formation of Si clusters), especially when monosilane (SiH_4) is employed as a precursor [16]. To minimize formation of Si clusters in the gas phase, addition of hydrogen chloride (HCl) or a chlorine(Cl)-containing precursor has shown successful results [17,18]. Growth at reduced pressure is also effective to suppress the Si-cluster formation [19,20]. By using these techniques, very high growth rates over 100 μm/h have been achieved. However, such fast epitaxy often results in formation of macroscopic defects such as in-grown stacking faults [21,22]. In recent years, Tsuchida and co-workers reported fast epitaxy of SiC by using high-speed rotation of a wafer holder, and they obtained very low density of stacking faults and other macroscopic defects below 0.5 cm^{-2} at a high growth rate of about 42 μm/h [23].

In bipolar devices, a heavily-doped p-type epitaxial layer is also necessary because injection of a high density of holes from the p-type layer into the lightly-doped voltage-blocking region is critical for achieving a low differential on-resistance. It is in general difficult to grow heavily Al-doped SiC by using the Cl-based chemistry [24] or on the C face [25].

A major remaining issue in SiC growth for fabrication of ultrahigh-voltage devices is stress control. Since the lattice constant is changed in heavily-doped SiC [26,27], significant stress may be induced near the p^+/n^- or n^-/n^+ interface. This is especially stringent when a very thick lightly-doped layer is grown on a heavily-doped substrate (wafer) with a large diameter. A large stress may lead to wafer warpage or generation of basal plane dislocations, both of which are detrimental for device production. Thus, a quantitative analysis of stress in epitaxial wafers and its control are important challenges.

2.2. Carrier lifetime

A carrier lifetime is a critical parameter, which determines the performance (on-state and switching characteristics) of bipolar devices, though it does not matter in unipolar devices. Fig. 3(a) depicts the forward current density – voltage characteristics simulated for 25 kV-