Materials Science in Semiconductor Processing xxx (xxxx) xxx–xxx

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Development, characterisation and simulation of wafer bonded Si-on-SiC substrates

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ARTICLE INFO

Keywords:
Silicon carbide
Wafer bonding
Si/SiC
Power electronic devices
Interfacial charge
MOS capacitors

ABSTRACT

Novel silicon-on-silicon carbide (Si/SiC) substrates are being developed in order to produce lateral power devices for harsh environment applications. Two methods of producing 100 mm Si/SiC substrates are detailed by wafer bonding silicon-on-insulator (SOI) wafers to semi-insulating 4H-SiC, then removing the SOI handle wafer and buried oxide. The final process includes a radical activation bonding process with low temperature processing, resulting in 97% yield. A uniform oxide layer at the Si/SiC interface of 1.4–1.8 nm is revealed, without voids, which minimises charge density at this interface. Capacitance-voltage (C-V) measurements of lateral metal-oxide-semiconductor capacitors (LMOS-Cs) are carried out on both processes revealing what appears to be an inversion from an n-type to a p-type like response in the 2 μm layers. Thinning the Si layers to 1 μm and making new LMOS-Cs, C-V responses show an improved n-type-like response, though frequency dispersion and incomplete accumulation remain. Finite element simulations showed that this effect could be reproduced by the introduction of interfacial charge at the two interfaces. Finally, while one possible explanation for fully inverting the C-V response of an n-type 2 μm Si layer on SiC was shown, the full understanding for this remains to be further studied.

1. Introduction

Silicon-on-silicon-carbide (Si/SiC) devices are being designed and fabricated for harsh environment applications [1–3] such as space. Designed to be both radiation hard and able to operate in extreme temperatures, devices are being targeted for power conversion applications such as electric propulsion [4] and high voltage transmission [5], where uncooled electronics could increase the overall lifetime, reliability, and science capability of a mission [6].

The Si/SiC substrate and device concept is shown [7–10] in Fig. 1. Lateral power MOSFETs and IGBTs, similar to the state of the art developed within SOI, are being developed to support 600 V within a 1 μm Si device layer. Unlike SOI, these substrates benefit from the high thermal conductivity and radiation hardness of the SiC, which allows for the efficient handling of self-heating effects. The wide bandgap of SiC forms both conduction and valence band offsets to the Si device layer, therefore minimising substrate leakage when using semi-insulating wafers. However, we have shown recently [7,8] that replacing the buried oxide in SOI with a SiC substrate leads to the loss of the double RESURF effect, and hence an increased series resistance.

Si/SiC substrates are herein formed by wafer bonding 100 mm semi-insulating 4H-SiC wafers to SOI wafers, before grinding down the SOI handle wafer and etching the buried oxide (BOX). Previously, the first groups to look into Si-on-SiC did so with a BOX between the layers, forming SOI wafers with a SiC handle wafer [11,12]. However, this is a methodology that our own modelling [9] proves to only fractionally impact on self-heating compared to conventional SOI. Si as a contact layer to SiC was considered using a SmartCut process [13,14] to transfer 400 nm of Si onto a 75 mm off-axis n-type 4H-SiC wafer, forming a heterojunction diode. Another method [2] involved the direct bonding of 50 mm Si and 6H-SiC wafers, before the Si wafer was ground and polished to approximately 1 μm. Simple lateral Si MOSFETs demonstrated the ability of the substrates to dissipate heat away from the junction region and maintain a high channel mobility at 300 °C. The use of SOI wafers in producing Si/SiC substrates was first proposed in [15], where a 330 nm device layer from a 100 mm SOI wafer was transferred

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http://dx.doi.org/10.1016/j.mssp.2017.10.020
Received 25 July 2017; Received in revised form 12 October 2017; Accepted 16 October 2017

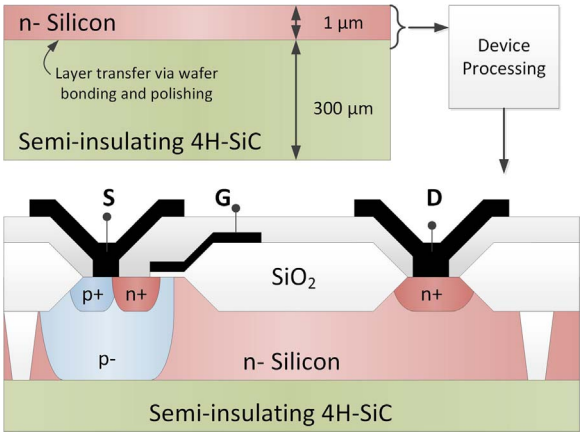

Fig. 1. Top, the Si/SiC material system that has been developed. Bottom, a proposed Si/SiC LD-MOSFET transistor.

onto a 50 mm 4H-SiC wafer, before removing the handle wafer. This was developed into a process [3] whereby a SIMOX SOI wafer with a 5 µm device layer was bonded to a polycrystalline SiC substrate with 800 nm of Si CVD grown on its surface. In this substrate, LD-MOS transistors were produced [3], which had an improved thermal and RF performance compared to SOI.

In this paper, we will discuss the development of 1 and 2 µm Si/SiC substrates that will be used for developing harsh environment LD-MOS devices. Using lateral MOS capacitors and FEM simulation, we will show the impact of interface charge on these layers and reveal how the bonding process was adapted to mitigate against this.

2. Experimental details

100 mm Si/SiC substrates have been produced with a Si device layer thickness of 1 and 2 µm, by two Bonding Processes (BPs). These are described here and illustrated in Fig. 2.

The starting material was common to both processes. A 100 mm Norstel semi-insulating (SI; ≥ 1.10^7 Ω cm) on-axis 4H-SiC wafer was to be bonded to a 100 mm IceMOS Technology Ltd SOI wafer with a buried oxide 2 µm thick, and a lightly n- doped device layer (5–45 Ω cm). These wafers were first cleaned using standard RCA cleaning solutions.

BP1 was carried out by IceMOS Technology Ltd and is extensively described in [10]. First, a grid of trenches 2 µm deep is etched into the SiC surface prior to bonding. This was designed as an escape route to for outgassing during the annealing process. The SOI device layer is etched to the final device layer thickness of 1 µm, if required. After a proprietary surface plasma treatment, a hydrophobic bonding process was performed to form a bond between the wafers. A 2 h, 1200 °C anneal was then performed to form a permanent bond between the wafers, and to shrink the interfacial oxide. This caused the wafers to bow, but as the Si handle wafer was ground away down to the oxide layer, this strain was released. Finally, the oxide, which had been the buried oxide of the SOI wafer, was removed with hydrofluoric acid.

BP2 was carried out by Tyndall National Institute, in which a radical activation process is used to enable low-temperature bonding. After RCA cleaning, a further cleaning process was performed using an EVG wafer-cleaning tool equipped with a DI megasonic nozzle. The wafers were then loaded in a bonder, in which the surfaces are exposed to nitrogen free radicals by an *in-situ* surface activation tool to improve the hydrophilicity of the surface prior to bonding the two wafers by bringing them into contact. The physical contact of the wafers forms a temporary bond. To enhance the bond strength the bonded pair was annealed *ex-situ* in N_2 ambient at 300 °C for 24 h. As in process 1, the SOI handle wafer was then thinned by grinding, before a HF solution was used to remove the buried oxide. An optional dry etch to reduce the

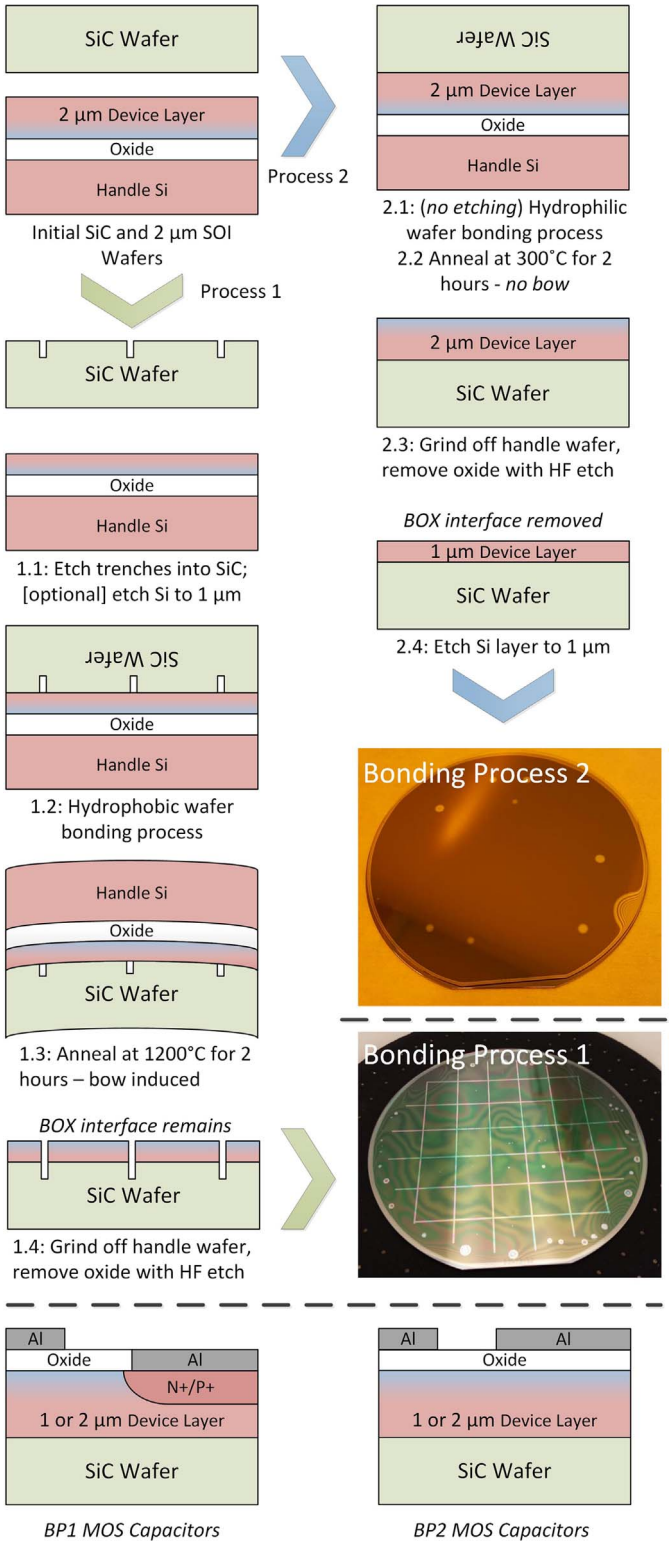

Fig. 2. Top: The two bonding processes described in the text, with images of the final bonded 100 mm Si/SiC substrates. Bottom: the two MOS capacitor structures used throughout.

device layer to 1 µm was then performed at the end of this process.

Laterally-contacted MOS Capacitors (LMOS-Cs) were formed on each Si/SiC substrate. These can be seen in Fig. 2. To fabricate the gate contact, the top Si surface was RCA cleaned before 55 nm of SiO_2 was thermally grown in dry oxygen (5 L/min) for 6 h followed by N_2O (1 L/min) annealing for 2 h, both at 900 °C. 300 nm Al was deposited as the