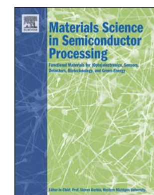
Materials Science in Semiconductor Processing 77 (2018) 83–87

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp



Effect of diffusion parameters on emitter formation in silicon solar cells by proximity rapid thermal diffusion

A. Oates, H.S. Reehal*

School of Engineering, London South Bank University, 103 Borough Road, London SE1 0AA, UK

ARTICLE INFO

Keywords:
Diffusion
Rapid thermal processing
Emitter formation
Silicon solar cells

ABSTRACT

N-type emitters have been formed in p-type monocrystalline silicon with good uniformity and high peak doping concentration by proximity rapid thermal diffusion (PRTD). High diffusion rates are achievable for relatively low temperatures (< 1000 °C) with the addition of O_2 to the N_2 diffusion atmosphere. Solar cells have been prepared from the diffused samples to assess their performance and efficiencies of up to 6.0% have been achieved. The devices possess high series resistance and high recombination rates amongst other factors which limit their performance. Reducing the junction depth improves Jsc and efficiency but is accompanied by degrading shunt resistance and FF for junction thicknesses below ~ 400 nm. Further refinements of cell processing should improve efficiency and result in a diffusion process for forming shallow emitters for application to microstructured devices such as micropillar radial junction solar cells.

1. Introduction

Silicon wafer solar cells dominate the solar PV market with ~ 90% market share [1]. The drive to reduce costs is targeting thinner Si wafers and more complex cell geometries including nano- and micro-wire designs with radial p-n junctions [2–4]. Formation of the p-n junction is a key stage in the cell fabrication process and is traditionally carried out in conventional thermal furnaces using solid or gaseous dopant sources. Ion implantation has also recently made inroads in PV manufacturing [5]. These techniques can have limitations in terms of control of junction depth and/or uniformity when applied to 3 dimensional structures such as micro and nanowire solar cells which require shallow junctions. Whilst ion implantation unquestionably permits fine concentration control and repeatability, it has a significant limitation when applied to 3D structured devices as complex tilt and rotation schemes are necessary to achieve uniform dopant distribution.

An alternative means of shallow junction fabrication is through the use of rapid thermal processing (RTP). Several RTP approaches including the use of spin on dopant (SOD) sources [6] or grown dopant oxides [7] deposited either directly on a sample to be doped [8], or on a sacrificial wafer acting as a solid dopant source [9], are reported in the literature. All have demonstrated the ability to form controllable, shallow junctions in silicon and indeed the directly applied SOD and grown oxide methods have been used to produce photovoltaic devices [10]. This approach, however, is potentially problematic for nano and microstructured devices due to the difficulty of applying conformal coatings of the dopant source to non-planar surfaces.

In this paper we concentrate on proximity rapid thermal diffusion (PRTD) as a means to fabricate shallow emitters with a view to doping micro-structured silicon solar cells [11]. This is a noncontact diffusion process that uses a sacrificial dopant source (referred hereafter to as a source wafer) prepared by spin coating a silicon wafer with a SOD. The source wafer is placed in proximity to samples to be doped. When heated, mass diffusion of the dopant from the SOD layer results. This is transported in the gas phase to the surface of the samples to be doped where adsorption and diffusion occurs [12]. By controlling the diffusion time and temperature it is possible to accurately control junction depths and dopant profiles [13].

There is little evidence in the literature of PRTD being used for the fabrication of solar devices. This paper presents results for PRTD diffused emitters in planar monocrystalline silicon solar cells. The aim is to develop the process to form radial junction micro-pillar solar cells.

2. Experimental

As supplied, p-type, 1–10 Ω cm, < 111 > orientated silicon wafers were used as dopant source carriers whilst 0.1 − 0.5 Ωcm, < 100 > orientated wafers were used as the substrate for diffusion. Prior to use they were subjected to a piranha clean process (3:1 – H_2SO_4:H_2O_2) to remove organic contamination, followed by rinsing with de-ionised water and drying in a steam of nitrogen.

Dopant source wafers were prepared by coating them with SOD; a

* Corresponding author.
E-mail address: reehalhs@lsbu.ac.uk (H.S. Reehal).

https://doi.org/10.1016/j.mssp.2017.12.006
Received 1 September 2017; Received in revised form 17 November 2017; Accepted 12 December 2017
1369-8001/ © 2017 Elsevier Ltd. All rights reserved.

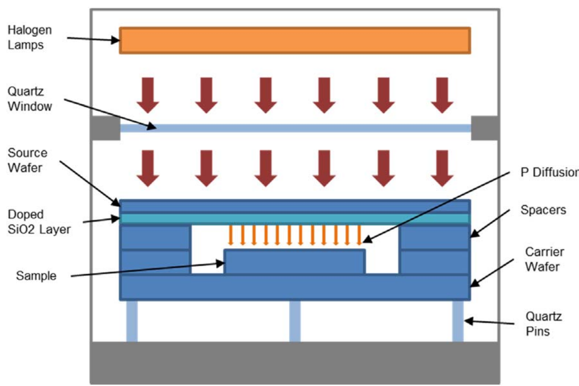


Fig. 1. Equipment configuration for proximity rapid thermal diffusion.

4 wt% solution of phosphosilicate polymer in a solvent carrier (supplied by Filmtronics). Different SOD concentrations were studied by diluting the as supplied solution with methanol. The solution was applied by spin-coating at 1000 rpm for 30 s to produce a uniform film. The wafers were then baked at 200 °C for 30 min in air to drive off residual solvent.

The samples to be diffused were prepared by cleaving the Si wafers into 13 × 13 mm^2 pieces. These were placed atop a Si wafer acting as a mechanical carrier in the RTP system (Fig. 1). The dopant source wafers were placed facing the samples using Si spacers to maintain a 0.5 mm gap between them. These were then loaded into the RTP system on top of a silicon carrier wafer. Silicon spacers were placed around the edge of the carrier before the source wafer was placed atop these to complete the diffusion stack. After loading, samples were subjected to diffusion processes with temperature varied in the range 770–1030 °C and a variety of cycle times.

The RTP system was an Annealsys AS-One 100 capable of supporting a 100 mm diameter wafer. It was pumped with a Varian SH-110 dry scroll pump. The diffusion was undertaken in an atmosphere of flowing electronic grade nitrogen (N_2) and oxygen (O_2). Typical thermal cycles for diffusions consisted of a fast ramp (< 60 s) to the peak diffusion temperature followed by a hold period which was varied in the range 1–15 mins. At the end of the hold period the temperature was ramped down to 500 °C over a short period ($\approx$ 180 s).

To analyse the depth of the junction produced, ball grooving and staining was used on selected samples. This technique consisted of forming a groove in the doped silicon substrate using a steel ball coated with a diamond paste to expose the diffused region and underlying substrate. A staining solution consisting of hydrofluoric acid, chromium trioxide and de-ionised water was then applied which created a visible contrast difference between the two regions. By measuring the radii of the two differentiated regions, combined with the known radius of the steel ball, the junction depth was calculated [14].

Solar cell fabrication was carried out as shown in Fig. 2. After diffusion and emitter formation, MESA edge isolation was performed by masking and wet etching the samples. Apiezon Wax W was used as the masking layer. Subsequently, a 1 μm thick layer of Al was sputtered onto the rear and annealed at 500 °C for 30 s in the RTP system to form an ohmic back contact to the p-type substrate. Front side contacting to the n-type emitter was achieved by sequentially evaporating bi-layer nickel-silver (15 nm and 1000 nm thick respectively) dots of 1.5 mm diameter around the edge of the front surface. The front contacts were annealed at 420 °C for 15 min in a tube furnace under nitrogen flow to form ohmic contacts. Finally, a transparent conducting oxide (TCO) layer of Al doped ZnO (AZO) was sputter deposited on the front surface to reduce front surface series resistance and complete the device structure. From the initial 13 × 13 mm^2 silicon pieces, the final cell size was 9 × 9 mm^2 after processing.

The cells were tested at 25 °C under AM1.5(G) illumination using a class A solar simulator and a Keithley 2400 Sourcemeter to sweep and measure the current-voltage characteristics. Four point probe measurements were used to map the sheet resistance of the diffused wafers. Additionally, the oxide layer thickness formed on the surface during the diffusion process was measured by ellipsometry to investigate the effect of the various diffusion parameters on its formation.

3. Results and discussion

The influence on diffusion of the SOD concentration, process gas flow rates and diffusion temperature was studied by measuring the oxide layer thickness formed during the diffusion process and the sheet resistance after the oxide had been stripped off in HF acid. Multiple 13 × 13 mm^2 samples were loaded into the centre of the RTP chamber during each run. The standard deviation of the average surface sheet resistance for each of the samples from a diffusion run, indicated by error bars in the figures below, was used an indicator of diffusion uniformity.

3.1. SOD concentration and N_2 flow rate

In PRTD, phosphorus from the SOD layer evaporates as phosphorus pentoxide (P_2O_5) and is transported to the silicon wafer substrate by gas phase diffusion. Adsorption and surface reaction processes lead to reduction of the dopant oxide and formation of a silicon oxide layer according to Eq. (1) [15].

$$2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2 \tag{1}$$

The phosphorus is incorporated into the oxide forming a phosphosilicate glass. This glassy layer then becomes the dopant source with phosphorus diffusing from this layer into the silicon by interstitial dopant diffusion, the primary means of phosphorus transport in silicon [16].

The influence of SOD concentration on sheet resistance and the

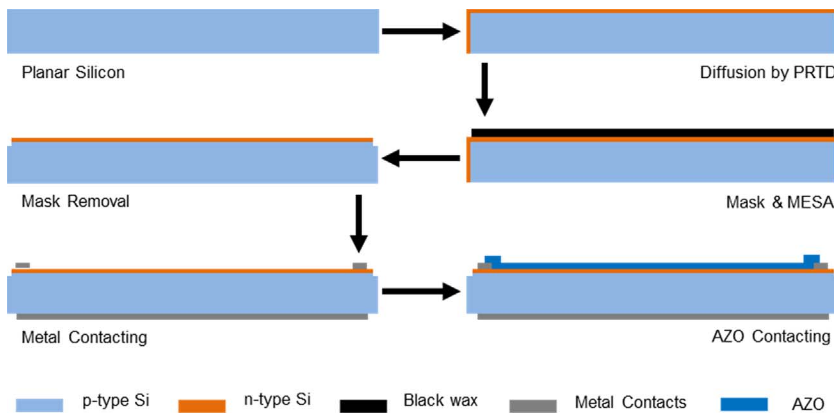


Fig. 2. Device fabrication steps with emitter formed by proximity rapid thermal diffusion.

Download English Version:

https://daneshyari.com/en/article/7117965

Download Persian Version:

https://daneshyari.com/article/7117965

Daneshyari.com