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A hybrid method of ultrafast laser dicing and high density plasma etching with water soluble mask for thin silicon wafer cutting

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ABSTRACT

Future silicon wafers are getting thinner in semiconductor industry to satisfy the requirement of miniaturizing package size in mobile device applications. Development of thin wafers is the mutual goal of current semiconductor researches. In this paper, a novel method incorporating the convenience of laser ablation and speed of plasma etching is proposed to replace traditional mechanical dicing saw for thin wafer cutting. The main idea is to use laser to create patterns on the silicon wafer coated with water soluble protection material and the unprotected area is exposed to the high-density plasma which is later etched through. This study includes development of the water-soluble protecting mask material, design of inductively coupled plasma (ICP) and microwave plasma sources, pattern scribing utilizing ultrafast laser, and trial of an etching (Bosch) process associated with the high-density plasma chamber to create high aspect ratio trench. The polyvinyl alcohol (PVA) based protecting material has excellent solubility and is extremely easy to be rinsed by water. With appropriately added chemicals, optical absorption is improved for laser ablation. A 532 nm 10 pico-second laser is used to perform surface scribing with minimal recast and heat affected zone (HAZ) at the edges. Good plasma homogeneity is demonstrated in the designed 12″ microwave and ICP chambers. With the protection coating the silicon wafer can be etched at 7.2 μm/min rate and 10.11 etch selectivity by the microwave and ICP sources in the chamber. Finally, etching process trials are performed, and the results show that deep and high aspect ratio trenches (~15 μm wide, ~95 μm deep) can be achieved which is fully acceptable for wafers under 100 μm thickness.

1. Introduction

Wafer dicing, also known as die singulation is part of integrated circuit package process to separate individual dies apart on a finished wafer for later packaging and assembly. Wafer dicing has been an indispensable front-end process for all integrated semiconductor devices namely, processors, memory, and radio frequency integrated circuit (RFIC) devices, as well as discrete semiconductor devices such as small-signal transistors, diodes, resistors, light emitting diodes (LEDs), solar cells, and microelectromechanical systems (MEMS) [1]. Significant portion of total package failure originates from defect during wafer dicing (e.g. cracking, bad edge quality) [2]. Future portable devices call for small, thin, and short size IC and the demand for thin wafer (less than 100 μm thickness) is increasing [3]. In the current era where electronic device is required to be small in size, low on cost but high on performance, the important role of thin/ultra-thin semiconductors bears no doubt. Thin wafers are poised to constitute about 50% of the overall semiconductors market in the few years to come. From their traditional thickness of about 500 μm, semiconductors are now available in ultra-thin variants with a thickness of about 40 μm [3]. Proliferation of thin wafer users and high adoption rate of portable devices are the major factors expected to drive thin wafer market growth. Increasing awareness coupled with expansion of semiconductor industry is expected to augment market growth over the forecast period [4] at a CAGR of 3.7% (between 2016 and 2022) and estimated to reach USD 9.17 billion by 2022 [5].

Thinner wafers help in reducing the thickness of whole packages (also the premises of stacked die), especially when it comes to mobile devices. Thinner wafers also efficiently assist good thermal management in electronic devices. All of these advantages act as growth driving force for the global thin wafers market. Furthermore, this rapidly reduction of wafer thickness will definitely create new challenges for the semiconductor industry including machining and handling. Ultra-thin wafers are more volatile as well as susceptible to damage under stress or cracking. The dies applied to thin wafers can break easily during the internal process or can break easily, which may hamper market growth over the next six years. However, these challenges can be overcome with wafer support systems, which are expected to mitigate these

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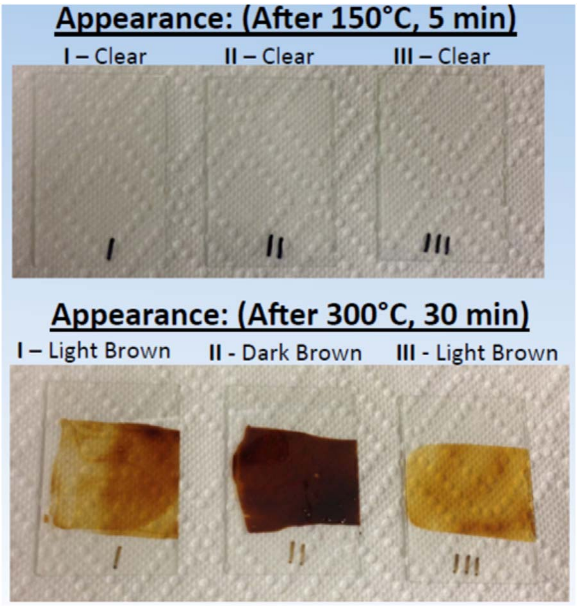

Fig. 1. Comparison of the three PVA compound samples after baking at 150 °C for 5 min and 300 °C for 30 min.

challenges by 2022 [5]. Mechanical dicing method cannot meet the

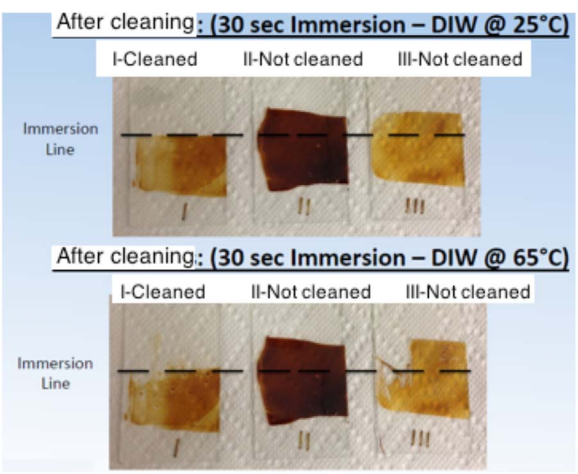

Fig. 2. Comparison of the baked samples after being immersed in deionized water at 25 °C and 65 °C for 30 s.

need of small cutting street and defect free zone in addition to the problem of stresses following the reduction of die size (< 0.2 × 0.2 mm) [6]. Traditional thin wafer production goes through a backside grinding before dicing (or vice versa) process. The disadvantages existing for small and thin dies are loss of strength and warping [7] due to grinding and burst-incision at cutting as the size drops to 0.2 × 0.2 mm.

An alternative means of wafer dicing is using laser technology, especially the ultrafast laser. The interaction between ultrafast laser and materials has been an interesting research topic in physical optics [8]. At different levels of laser irradiation, the optical reaction with materials can be drastically different, in addition, optical absorption depends on the wave length. Within ultrafast time scale e.g. pico or femto second, the peak laser pulse power can be extremely high and exceed the non-linear absorption threshold. A highly focused ultrafast laser

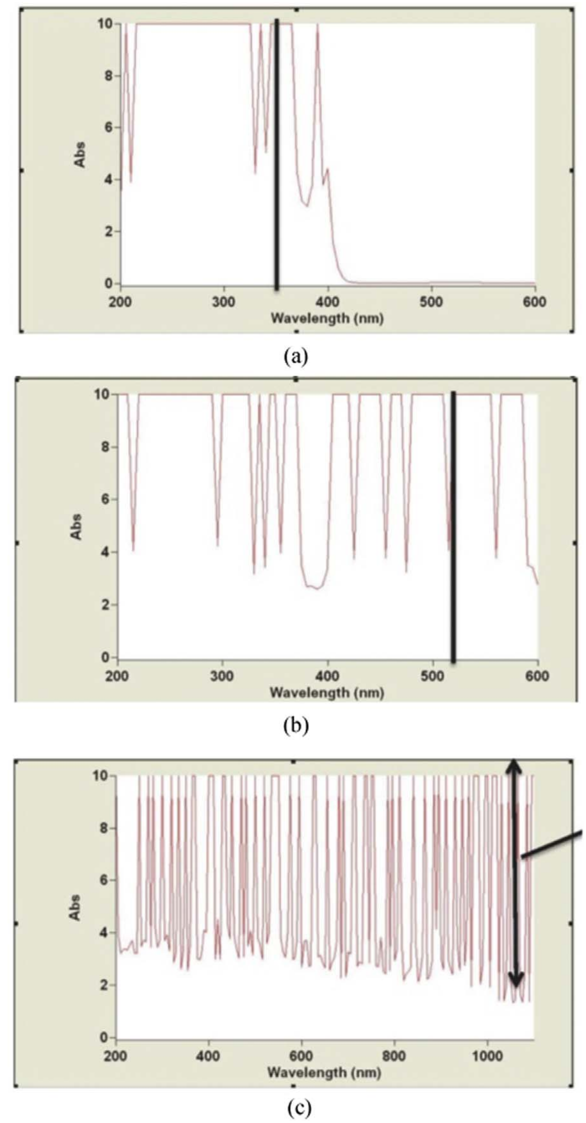

Fig. 3. The optical absorption spectra of the e-Ray Optoelectronics GAN3 compound: (a) 355 nm (b) 532 nm and (c) 1064 nm. (The values on the vertical axis are in arbitrary unit for comparison only.).

beam can create a very clean lesion at the focal point i.e. a near "cold" ablation with minimal heat affected zone (HAZ) [9-12], not only in transparent materials such as silicon and sapphire but also opaque metals. Laser may be a promising tool for cutting finished silicon wafers with embedded low-k and Cu layout which is one of the most rigorous problem for lithography process [9,10]. Single pass laser scribing can be completed on the fly. However, the processing rate of laser full cutting is limited by the speed of the traverse mechanism and necessary multi-pass laser irradiation especially when large 12″ wafer is processed. Combination of novel polygonal scanner and x-y stage [11] can help to reach higher speed for full cutting of thin wafers. However, it suffers a few inherent problems: 1. limitation of scanning range 2. shifting of focal depth and 3. field distortion at the ends of ranging. Dice-and-break may be the most feasible way for laser cutting, even though, the breaking process entails stress problem and new failure mode.

Yet another technology which can be applied in thin wafer singulation is the plasma etching [13,14]. Deep reactive ion etching (DRIE) is