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Stress-induced trench narrowing in Cu interconnect of sub-20 nm node: FEM simulation

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ABSTRACT

The trench narrowing at sub-20 nm BEOL process has been reproduced using a FEM simulation. The trench narrowing can be observed under the conditions of both the high intrinsic stress of a hard mask and the specific design of metal line patterns with the length difference between center and side trenches. As the center trench length increases, a trench displacement takes place because trench walls have a high compressive stress gradient from the side trench surface to the center one in the direction parallel to the trench lines. The displacement also decreases with decreasing the width of the trench while increasing with decreasing the width of the low-k wall. The high pattern density of metal or dummy lines around the trenches decreases the displacement of the low-k dielectric walls. Considering the distribution of pattern densities at left and right sides of the trenches, a symmetrical pattern density deforms the trench wall more largely than an asymmetrical one. Young's modulus of SiOCH is not a sensitive factor on the trench narrowing. Our displacement analysis may be used in predicting hot spots of void defects in the Cu interconnect of real Si wafers.

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1. Introductions

In semiconductor industry, sub-20 nm silicon process has been recently introduced, and such a small scale gives rise to many challenges in process yield and reliability. Since elastic modulus, melting temperature, and yield strength dramatically decrease as a particle or a grain size drops below ~20 nm [1–3], materials may be easily damaged and deformed by heat and mechanical stress during fab process. It is, thus, of critical significance to deeply understand how materials response to heat and mechanical stress in order to maintain excellent process yield and reliability in fabricating highly integrated devices. Particularly, the heat and mechanical stress need to be carefully considered in BEOL (Back End of Line) process since having been root causes of process and device failures.

There have been many thermal or mechanical stress issues in BEOL process [4–13,16,17]. Thermal expansion difference in between a low-k dielectric and a Cu metal often causes mechanical stress issues: KOZ (Keep-Out Zone) in TSV [4,5] and a mechanical fracture using ultra low-*k* material in a BEOL stack [6], etc. There are also residual stress problems (delamination [7], buckling [8,9] and fracture [10]) produced by deposited films such as TiN, Si_3N_4 and W. While tungsten [11] and silicon nitride [12] usually have high tensile stress more than 1 GPa, titanium nitride [11] shows high compressive stress more than 1 GPa. Darnon et al. [8] reported the undulation of a sub-100 nm dielectric structure by a TiN metal hard mask (MHM). Stan et al. [9] also suggested the analytical model that quantitatively describes the morphologies of the buckled fins during hard-mask patterning. The deformation of a dielectric film has been also found in the BEOL process of sub-30 nm node using the TiN MHM. Furthermore, a trench narrowing or a closure occurred by the displacement of a dielectric oxide at the trench structure. The trench narrowing often results in a void due to the difficulty of Cu filling during metallization [13,16]. Torazawa et al. [13] investigated the displacement of a failure pattern using FEM and suggested film properties to minimize the residual stress of a TiN film. Kaulfersch et al. [16] reported parametric study results of geometric variation at the trench narrowing using a symmetrical pattern structure.

In the present work, the mechanism of trench narrowing is basically revealed by analyzing the deformation response of a dielectric structure to the intrinsic stress of TiN. The trench narrowing is examined with geometric factors of patterns such as a length difference between trenches and widths of a trench and its low-*k* wall. Particularly, since silicon process is being integrated

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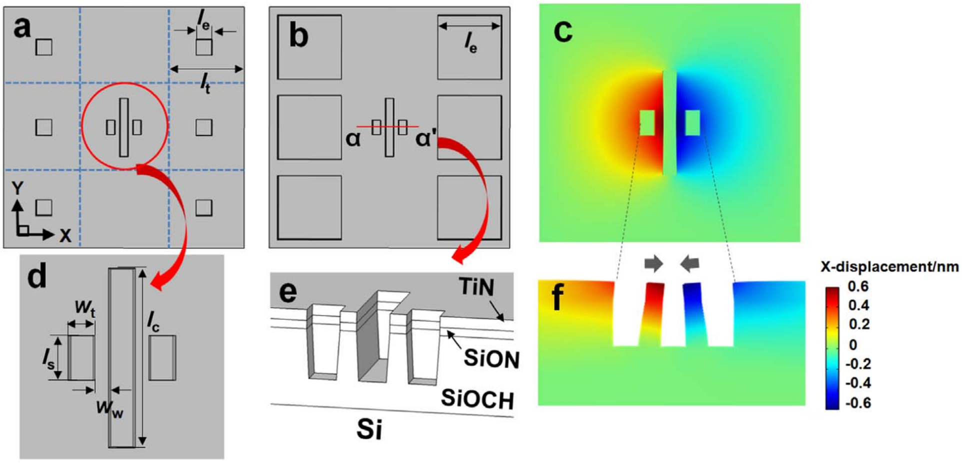

Fig. 1. Schematics of a simulation cell structure. a. There are three trenches at a center of the simulation cell. Six squares around the trenches are empty spaces, and considered as a simplified pattern density: a and b indicate a low and a high pattern density around the trenches, respectively. c. A 2D image of displacement at a top surface after simulation. Blue and red colors indicate directions of the displacement: red shows the displacement occurs to the x-direction. d. Geometrical variables of the tranches e. A vertical stack (side view). f. A 2D cross-sectional view at α-α′ of b. Small gray arrows denote the displacement directions of trench walls. Whereas the color shows real displacements from our simulations, deformation of the trench shape is increased 20 times at the images of c and f to see the trench narrowing easily. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

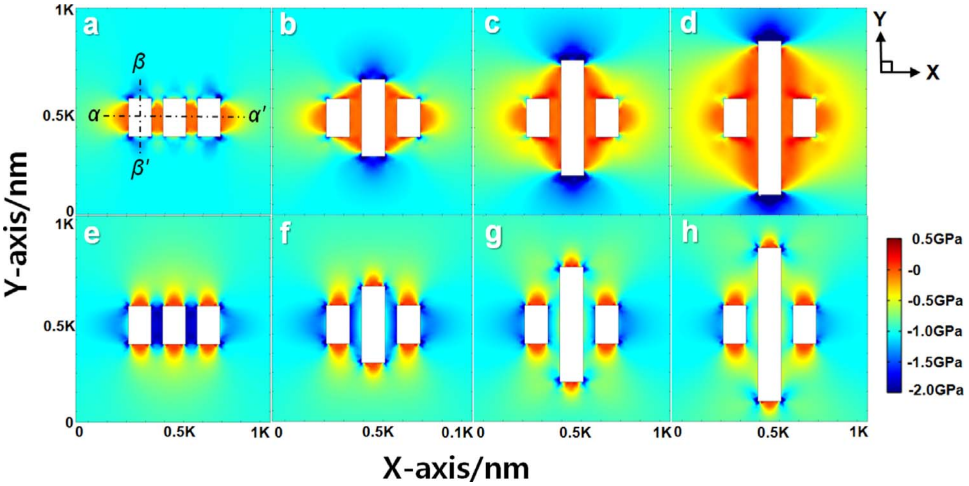

Fig. 2. 2D distribution maps of σ_{xx} and σ_{yy} at three trenches: a–d. σ_{xx}, e–h. σ_{yy}. a and e. $\delta=0$, b and f. $\delta=1$, c and g. $\delta=2$, d and h. $\delta=3$. Each image shows x- and y-stress on TiN surfaces. The length of the center trench (l_c) is changed with the TiN residual stress of 1 GPa.

toward sub-10 nm node, the width of the inter-trench walls will decrease as a necessity. The relation between the pattern geometry and the trench deformation behavior needs to be thus addressed to avoid potential pattern failures at BEOL process. We also look into how the trench narrowing is affected by material properties (e.g. the intrinsic stress of TiN and the elastic modulus of low-k material, SiOCH). Our results will provide understanding of the relation between physical causes (stress and material properties) and a pattern design of Cu interconnects to minimize overall failures by the dielectric displacement.

2. Simulation approach

The COMSOL software is adopted as a simulation tool for FEM simulations. The trench structures for this work are illustrated in Fig. 1. The simulation structure is made of 9 sub-cells as divided with a blue dot line in Fig. 1a. The center cell has three trench lines, and each of 3 cells at left and right sides has an empty space considered as a simplified trench of real metal patterns. The six empty spaces are used to examine a density effect of neighboring trenches (see different neighboring trench densities at Figs. 1a and b). l_t and l_e denote the sizes of the sub-cell and the empty space, respectively. l_e/l_t is defined as a local empty ratio, and the total empty ratio (ρ) is obtained by averaging the local empty ratios of the left and right sides. In Fig. 1d, l_c and l_s are the lengths of the center and the side trenches, respectively. The length difference, δ, between the center and the side trenches is defined as $(l_c-l_s)/l_s\times 100$. w_t and w_w are also represented as the widths of the trench and its side wall, respectively. Since the trench narrowing is experimentally found before metallization of Cu, the simulation structure consists of TiN, SiON, SiOCH layers on Si without a barrier metal and Cu as illustrated in Fig. 1e. Film thicknesses of TiN, SiON, and SiOCH are set to be 20, 15, and 140 nm, respectively. Intrinsic (or residual) stress of -1 GPa, experimentally measured, is basically applied parallel to the TiN film surface, and changed from 0 to -1.5 GPa to examine a stress-dependency of the trench narrowing. The cell is fixed at boundaries of a bottom and sides, and free at a top surface during simulation. All simulations are conducted at 293 K. As shown in Fig. 1c and f, our simulation set-up reproduces the trench narrowing previously reported [13,16].

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