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Mechanism and detection of poly gate leakage with nonvisual defects by voltage contrast inspection

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ABSTRACT

The research aims at nonvisual defects causing the poly gate leakage failure and the corresponding inline voltage-contrast (VC) inspection. Electron beam inspection (EBI) begins to be frequently used for scanning either SRAM or DRAM cell area in nano-scaled technologies. The research, furthermore, extends EBI to logical area of an ASIC product and proposes an inline detectable methodology for gate leakages. Extreme tiny and nonvisual residues could happen during gate etch processes by the step height between active area (AA) and shallow trench isolation (STI), and the tiny defects are difficult to be located even some of those did lead to chip probe (CP) test failure. The subsequent implant processes would punch through those tiny poly residues, make the residue being conductive, and finally electrons on the gate would leak to the ground through the residue. Those nonvisual residues act as bridges for gate leakages. EBI with designed positive charging modes was applied into the series of implement steps and found the leakage by a significant voltage contrast signal post the source/drain implantation. The bright VC of the gate poly implied the leakage electrons charging on the gate. A series of process experiments based on the model for reducing leakages was tested and quickly verified by the EBI in front end of the line. An optimal process integration condition was soon carried out with a significant chip yield enhancement.

1. Introduction

With superior resolutions and voltage contrast features, electron beam inspection begins to being frequently used while technologies entered nanometre scale. The applications of EBI have been widely studied on dense cells of DRAM [1], SRAM [2–4] and flash ram [5]. The common practice is to scan the wafer post contact tungsten (W) chemical and mechanical polish (CTW CMP) [6]. CTW CMP layer, with CMP making a flat surface and conductive W plugs surrounding by oxides, discriminates in favour of EBI. The bright or dark voltage contrast related to underneath open or short for electrons can be achieved on top of W plugs and, in doing so, many of device failure issues can be early reported ahead the end-of-the-line chip test.

Via EBI in the-middle-end-of-the-line (MEOL) CTW CMP layer, VC inspection can identify electron leakage via NiSi spiking in the vertical direction [2] and breakdown of intra-well isolation in the lateral direction [3]. Advanced semiconductor process lines tend to require more e-beam scans, especially in the early phase of technology development. SRAM, a common process development vehicle [7], is suitable for electron beam scanning for in-process detection that shortens the development time. Besides product chips, EBI has been used in a dedicated sweep test for routine monitoring of line defects [8]. These typical applications detected physical defects, either very small surface or open/short subsurface defects. Here we extend VC inspection to detect leakage, an important electrical parameter for devices. Surface VC charging by an electron signal potentially can identify process incoherence for those critical layers; e.g., contact and poly, which is only revealed by end-of-line functional tests by traditional approaches.

In this paper, a novel EBI methodology for inline detection of gate leakage in the logical area was presented. The methodology allowed the inspection performed in FEOL; instead of MEOL, the nonvisual defects were quickly addressed and fixed with instant verification. The nonvisual tiny residue caused gate leakage was addressed, and the failure mechanism was described. The VC signal varies following multi implementation layers are traced, and source/drain (S/D) implantation was the last straw breaking the camel's back that provided a breakthrough-point dosage for the leakage. The solution of inline process optimization on reducing the step height between AA and STI and extending of poly etch was figured out, and the yield then jumped 9% up. The methodology, comparing with end-of-line wafer chip probe (CP) test,

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provides a tremendous time advantage for evaluating repeating experiments and speed up yield enhancement.

2. Inline voltage contrast inspection

2.1. Low yield with leakage failure bins

In the initial stage of volume production of an ASIC (Application Specific Integrated Circuit) product in a 300 mm fab, a repeating low yield issue with leakage related bins was reported by the end-of-line CP test. The map distribution of the failure chips, as shown in Fig. 1(a), was a shape of donut at both wafer center and edge. With the failure bin corresponding modules, an area contented logical circuits was marked as shown in Fig. 1(b). And that's it; the information is far from enough to address the exact failure location in the nano-metre world. Even the reverse engineering had been executed; the delayering PFA (physical failure analysis) did not find abnormality in the logical block. This is a continual suffering event; however, the traditional analysis method cannot address the cause. Each of inline and end-of-the-line parameters, involving WAT (wafer acceptance test), process commonality, CD (critical dimension), thickness, and etc. were pull out and checked. All process parameters were under control, and the defect source cannot be found.

This kind of CP failure cases difficult for finding the root cause are not rarely in semiconductor manufacture, since it's challenging for addressing defects in logical area of an ASIC, especially in foundry fabs.

2.2. VC inspection post CTW CMP

It's difficult to identify inline process step or interval as defect source only by the end of the line leakage failures of CP test. There are many possible causes through all processes that could lead to leakages; for instance, BEOL metal or via leakage with inter-metal dielectric, MEOL contact leakage between the 1st metal layer and device, FEOL AA and gate poly leakage within the device, and etc. many processes through the line all could result in similar failures.

The VC feature of EBI can represent for various kinds of leakage issues by physical defects. Since the leakage was found till the end of the line, EBI was used to examine through the processes reversely to top metal, inter-metal, the 1st metal layer and CTW CMP. Furthermore, alternative scan modes with both positive and negative surface charging were adopted to perform duplicate scans for the various and complicated VC appearances of the logical circuits. Through a wide-ranging and deep-reaching inspection, the scan result in CTW_CMP showed the similar distribution to the failure CP map. Fig. 2(a) is the defect map that presented a donut shape similar to the CP map in Fig. 1(a). The low yield map of Fig. 1(a) is center and top-right while Fig. 2(a) is center and bottom-right area. The failure maps to maps showed in rotation, and which was related to the gate etch process with wafer to wafer small angle rotation. To zoom in the defect point with SEM as showed in Fig. 2(b), three adjacent abnormal contacts were found. The three contacts comparing to normal chips supposed to be "bright" but showed "dark". To sort the underneath structure and layout as shown in Fig. 2(c), the three contacts all land on one poly line which cross over N and PMOS. Gate poly lines are floating with oxide insulating to the silicon ground and, for the VC, the electrons should be accumulated with "bright" appearance. The three "dark" contacts imply the underneath poly line short to the ground and leakage happened.

The contacts on NMOS landed on N+/P-well, and electrons in the bulk cannot flow up to the surface of the contact through the NP junction. Therefore, VC of contacts on NMOS is dark. The contact on PMOS is vise verse and VC is bright. Since VC on NMOS is dark but on PMOS is bright, the poly line across N/PMOS and cause the contacts turned dark should have problem on the end of NMOS. However, the cross-section cuts of that suspected-leakage poly line at NMOS showed normal in all directions. Even the delayer physical failure analysis was executed and the poly was removed, it was difficult to figure out the leakage source. Fig. 3 (a) shows the smooth surface of the poly shape, however, there is a very small break on the round spacer nitride. The high resolution TEM image, as shown in Fig. 3(b), reveals a tiny residue buried in the spacer, which is nearly invisible but could be the cause for the leakage.

2.3. FEOL VC inspection

EBI had found leakage contacts in middle end of the line at CTW and shorten the response time from end of the line. However, the defect is still underneath and cannot be observed directly. FEOL VC inspection thus was tested to get even closer to the leakage source.

That poly line under the three dark contacts was targeted, and step-by-step inspection was carried out during the formation of the poly line and subsequent processes. Fig. 4 shows VC images captured following different process steps and summarized as below:

(1) The shape of the poly line is well defined. The observation since lithography to poly etch (see Fig. 4(a)) showed the geometry of the poly line is accurate and normal.
(2) VC enhanced following implantation processes. Between poly and spacer etch, many lightly doped drain (LDD) implantations are applied into P and NMOS, respectively. Fig. 4 (b) shows strong VC signal that grounded AA (active area) source/drain is bright and floating gate poly line is dark.
(3) The "bright" poly found after NP implantations. One of the poly lines became bright and supposed to be grounded as shown in Fig. 4(c).
(4) The leakage happened on the three contacts with dark VC. Electrons would leak through those the three contacts and the grounded poly line into the substrate, and which result in dark

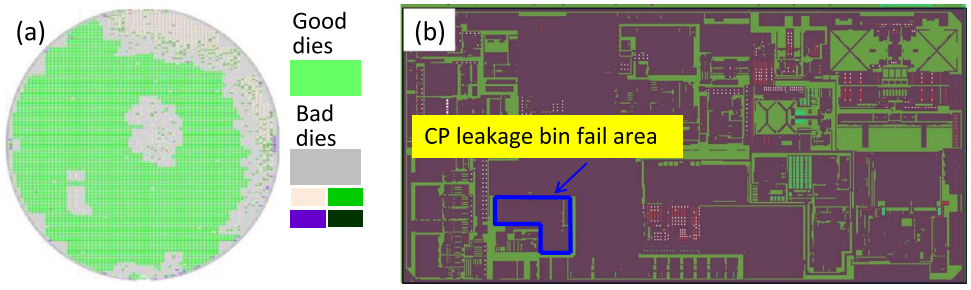

Fig. 1. (a) CP yield map and (b) the leakage bin corresponding area within the chip.