Materials Science in Semiconductor Processing 40 (2015) 896–909

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Review

Atomic-scale tomography of semiconductor nanowires

Jiangtao Qu [a], Simon Ringer [b,c], Rongkun Zheng [a,*]

[a] School of Physics, The University of Sydney, New South Wales 2006, Australia
[b] Australian Centre for Microscopy & Microanalysis, The University of Sydney, New South Wales 2006, Australia
[c] School of Aerospace, Mechanical and Mechatronic Engineering, The University of Sydney, New South Wales 2006, Australia

ARTICLE INFO

Article history:
Received 30 July 2015
Accepted 31 July 2015

Keywords:
Atom probe tomography
LEAP
APT
Semiconductor nanowires
Specimen preparation

ABSTRACT

Atomic-scale structure and composition is critical to understand the novel properties and to realize the technological applications of semiconductor nanowires. This paper reviews the latest progresses in atomic-scale tomography of various semiconductor nanowires for application in electronics, photonics, thermoelectrics and photovoltaics. In practice, specimen preparation is usually the obstacle for the atomic-scale tomographic experiment. In this regard, promising specimen preparation methods from semiconductor nanowires are also summarized and compared. The unprecedented information extracted from 3D reconstruction of tomographic data provides deep insight into semiconductor nanowires and enables understanding of properties and optimization of growth.

Contents

1. Introduction

For the sake of performance improving and cost cutting of integrated circuits commercially, the feature size of transistors has been driven to scale down continuously for more than 50 years as predicted by Moore's Law and the availability of the products on market made by Intel's latest 2nd generation 3D tri-gate 14 nm transistors assure that the promise of Moore's Law will continue to be fulfilled this year [1]. Although extraordinary progress has been made, there are still lots of challenges if the performance of chips is expected to have further improvement involving mobility degeneration and further miniaturization [2,3]. However this seems an impossible task with traditional silicon technology due to physical limitation and severe short channel effect (SCE) [4–18] as the scaling-down continues.

Therefore, new transistor architectures and new materials are desired to boost the IC performance with further scaling-down [19,20]. Semiconductor nanowires have demonstrated wide potential applications with respect to their unique properties [21–24] and possible compatibility with current processing technology,

* Corresponding author. Postal address: School of Physics, Madsen Building F09, The University of Sydney, NSW 2006, Australia. Fax: +61 0293517682.
E-mail address: rongkun.zheng@sydney.edu.au (R. Zheng).

http://dx.doi.org/10.1016/j.mssp.2015.07.093
1369-8001/

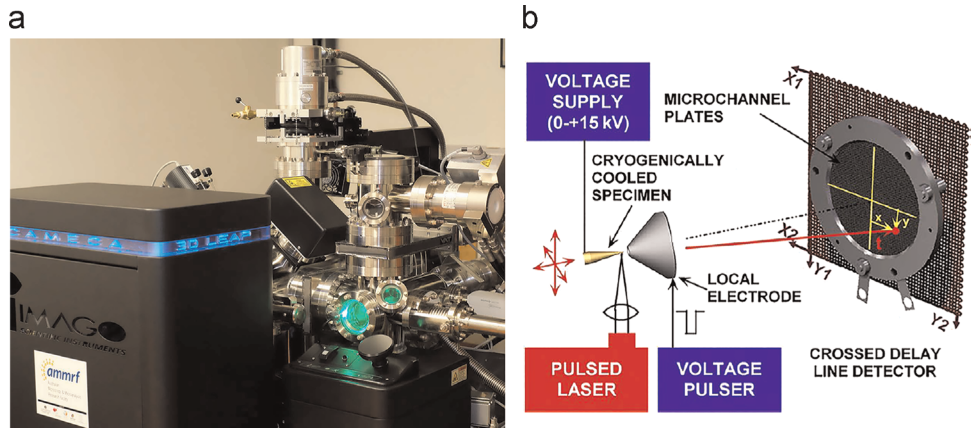

Fig. 1. (a) Image of Cameca LEAP 4000XSi. (b) Schematic diagram of a local electrode atom probe (LEAP) with a crossed delay line single atom detector at the end of the time-of-flight mass spectrometer. Both voltage and laser pulsing modes of field evaporation are shown [46].

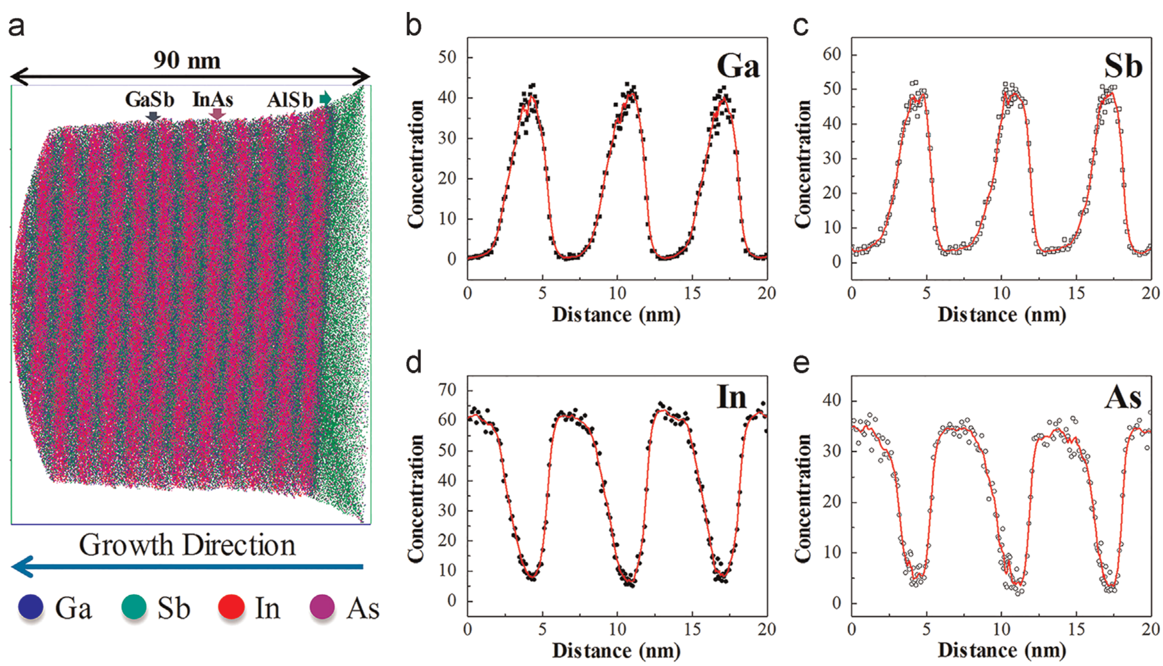

Fig. 2. (a) 3-D reconstruction of InAs/GaSb superlattice near the substrate region obtained using atom-probe tomography. Concentration profiles for: (b) Ga; (c) Sb; (d) In; and (e) As across the interfaces, showing asymmetric interfacial chemical sharpness [55].

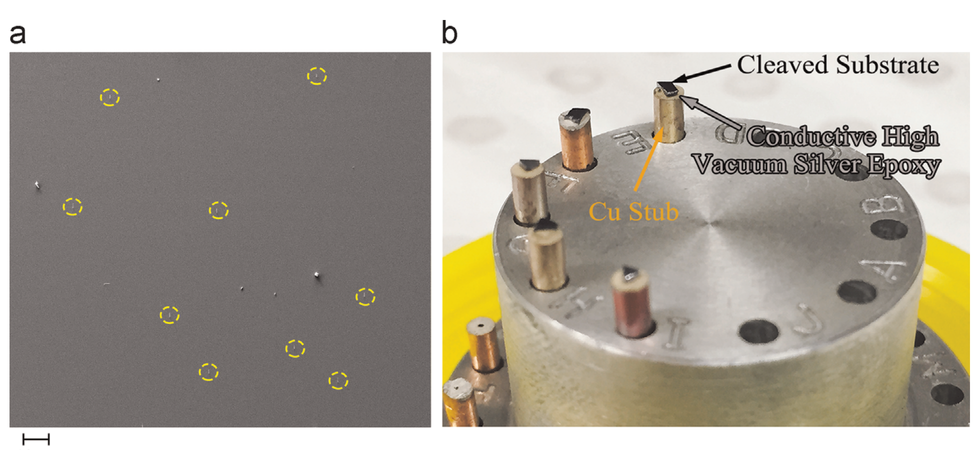

Fig. 3. Low density GaAs nanowires specimen for APT.