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# GaAsP on SiGe/Si material quality improvements with in-situ stress sensor and resulting tandem device performance

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ABSTRACT

GaAsP solar cells have been grown on Si substrates facilitated by a SiGe graded buffer layer. Materials-based characterization demonstrates threading dislocation densities (TDD) as low as $8.0 \times 10^6$ cm$^{-2}$ via cathodoluminescence in III–V layers from dual-junction solar cells. The difference in material quality and device performance between lattice-match conditions at room temperature and growth temperature are quantified. These improvements are primarily realized through the use of an in-situ optical stress sensor in order to evaluate lattice-mismatch during MOCVD growth. Thus, due to improved material quality, window layer design, and contact resistance, we have achieved GaAsP/SiGe tandem performance with an AM1.5G open-circuit voltage of 1.458 V, a top subcell external quantum efficiency-extracted short-circuit current density of 13.8 mA/cm$^2$ (no AR), and a fill factor of 82.8%.



## 1. Introduction

The highest efficiencies in photovoltaics are provided by III–V devices [1]. However, these devices incur high costs because they require lattice-matched substrates and metal organic chemical vapor deposition (MOCVD) operation and device development, making them prohibitively expensive in many markets. This cost can be reduced by utilizing silicon substrates and limiting the thickness of the III–V MOCVD material growth.

Nevertheless, developing III–V layers on Si substrates involves considerable complexities. Perhaps the greatest challenge is lattice-mismatch. Si has little in the III–V material system that is close to its lattice constant. Thus it requires a graded buffer region to shift the lattice constant while still maintaining low threading dislocation density (TDD).

This initiative plans to leverage the technology of a metamorphic silicon:germanium (SiGe) buffer [2] that lies between the silicon substrate and the active device layers. Developed by AmberWave Inc., this buffer provides a low-dislocation interface for III–V nucleation and a high quality bottom cell that is grown by reduced pressure chemical vapor deposition (RPCVD) [3].

Previously we presented calculations for a modified Shockley–Queisser [4] evaluation of III–V/SiGe lattice-matched tandem solar cells [5]. We identified an ideal III–V top subcell ternary material, gallium arsenide phosphide (GaAsP), and provided a direction for initial experimental work.

This paper characterizes the materials and details the device development of GaAsP/SiGe on Si tandem solar cells with an emphasis on the material quality of III–V layers.

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First, the growth conditions and material characterization are discussed. Next, research on GaAsP/SiGe tandem solar cells is described that focuses on the evaluation of lattice matching III–V layers to the underlying final SiGe composition at growth temperature. This is accomplished using an in-situ stress sensor to quantify the stress incurred during III–V epitaxial growth. Finally, we conclude by discussing the best pathways for near-term improvements in these devices.

## 2. Background

III–V devices are often parameterized over a wide range of bandgaps (Eg) using the bandgap-voltage offset ($W_{oc} = Eg - V_{oc}$) [6], a technique that is particularly suited for comparing the various direct bandgap III–V on Si solar cells from literature since the metric is relatively invariant with respect to bandgap and highly sensitive to fluctuations in saturation current.

The concept of developing a III–V top cell on a Si substrate is not new; many researchers have developed initiatives in the past. Most results suggest that material quality is the limiting factor in device realization as shown by TDD values. To support this statement, we provide below an overview of independent literature results.

Early III–V on Si work was largely focused on GaAs devices utilizing a thermal cycle anneal technique (TCA). Initial research using this technique at NTT Electrical Communications Lab [7,8] reported that increasing the thickness of a GaAs buffer layer decreased the TDD. These researchers demonstrated a best device that offered a $W_{oc}$ of 0.51 V with a TDD as low as $4.0 \times 10^6$ cm$^{-2}$ measured via etch-pit density (EPD) and transmission electron microscopy (TEM). Using the same techniques, Spire Corporation achieved similar results, a $W_{oc}$ of 0.53 V at $8.0 \times 10^6$ cm$^{-2}$ TDD [9,10].

A technique of GaP nucleation with GaAsP graded buffer was used by Geisz et al. [11] and Grassman et al. [12]. Geisz et al. achieved an AM1.5 efficiency of 9.8% with a $V_{oc}$ of 0.985 V ($W_{oc}$ of 0.73 V). They reported a TDD of $9.4 \times 10^7$ cm$^{-2}$ measured via electron-beam-induced current (EBIC). More recently, GaAsP has been grown on a GaP/Si template using a GaAsP metamorphic buffer, achieving TDD values of $0.99 - 1.3 \times 10^7$ cm$^{-2}$ via EBIC [13]. This resulted in a $W_{oc}$ equivalent to 0.59 V for both n+/p and p+/n structures.

In 1995, Soga et al. [14] achieved single-junction and tandem results using TCA and a GaAs nucleation grown by MOCVD. Soga grew a 1.55 eV AlGaAs device on the GaAs nucleation, and in doing so, took advantage of the minimal lattice-mismatch incurred by adding Aluminum to the GaAs material system. Their single-junction device achieved a $W_{oc}$ of 0.62 V and a TDD of $1.1 \times 10^7$ cm$^{-2}$ via EBIC.

The use of SiGe as a graded buffer has also been seen in other research endeavors. Andre [15] used the SiGe graded buffer on Si and demonstrated growth of single-junction GaInP with a $W_{oc}$ of 0.57 V and a $7 \times 10^6$ cm$^{-2}$ TDD via EBIC. Research related to Andre's work led to the best reported device, a single-junction GaAs device on a SiGe graded buffer that achieved 0.45 V $W_{oc}$ at $0.8 - 1.5 \times 10^6$ cm$^{-2}$ TDD via TEM, EPD, and EBIC in the Ge cap layer [16]. In this device the SiGe grades fully from the Si substrate to an almost 100% Ge layer.

These $W_{oc}$ values appear to be a function of TDD. This suggests that the limiting mechanism for these devices is TDD-based recombination. In support of this idea, many researchers, such as Yamaguchi et al. [8], have suggested that better results can only be attained by improving the TDD.

## 3. Experimental growth and characterization

### 3.1. SiGe on Si

The SiGe layers were grown at AmberWave Inc. in a RPCVD reactor on (100) 6° offcut to the <111> CZ silicon. For the devices discussed in this paper, buffers were grown to final compositions of 82% Ge (approx. 0.86 eV indirect bandgap). This final composition was chosen because previous calculations [5] predicted that this tandem bandgap combination was near the current match between GaAsP and SiGe and therefore the optimized AM1.5G architecture for this material combination. The grade was accomplished in under 5 μm of epitaxy, thus allowing for further III–V growth without reaching the cracking limit [17]. EPD showed that up to 88% Ge SiGe yields a TDD of $3 \times 10^5$ cm$^{-2}$ [3]. After the graded buffer, a low-doped SiGe cap layer was grown at the final structure composition.

In earlier research, a single-junction SiGe solar cell was developed on this graded buffer [18]. This produced $Si_{.12}Ge_{.88}$ (approx. 0.82 eV indirect bandgap) devices with a $V_{oc}$ equivalent to 261 mV at 1-sun below a Si filter. Separately, the use of a textured back reflecting mirror increased the optical path length 17x over a planar SiGe design, facilitating a significant current boost in the solar cell [19].

### 3.2. III–V on SiGe

III–V growth was completed at Veeco MOCVD using a Veeco K475 As/P MOCVD tool. Precursors used in the epitaxial growth process include phosphine ($PH_3$), arsine ($AsH_3$), trimethylgallium (TMGa), dimethylzinc (DMZn), trimethylindium (TMIn), disilane ($Si_2H_6$), carbon tetrabromide ($CBr_4$), and diethyltellurium (DETe). $PH_3$ hydride was initiated at 400 °C during the initial MOCVD temperature ramp. III–V layer growth was maintained at 640 °C with the exception of tunnel junctions which are grown at 580 °C. Initial nucleation tests established that gallium indium phosphide (GaInP) provided better nucleation quality since GaAsP nucleation layers demonstrated lower in-situ measured reflectance and greater wafer bowing. GaInP and GaAsP layers were grown under high V/III ratios of 122 and 45, respectively.

Using x-ray diffraction (XRD), we found that 20% P GaAsP (approx. 1.66 eV) lattice-matched with 82% Ge SiGe at room temperature.