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Source/drain metallization effects on the specific contact resistance of indium tin zinc oxide thin film transistors

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A B S T R A C T

We report on the specific contact resistance of interfaces between thin amorphous semiconductor Indium Tin Zinc Oxide (ITZO) channel layers and different source/drain (S/D) electrodes (Al, ITO, and Ni) in amorphous oxide thin film transistors (TFTs) at different channel lengths using a transmission line model. All the contacts showed linear current–voltage characteristics. The effects of different channel lengths (200–800 μm, step 200 μm) and the contact resistance on the performance of TFT devices are discussed in this work. The Al/ITZO TFT samples with the channel length of 200 μm showed metallic behavior with a linear drain current-gate voltage (I_D–V_G) curve due to the formation of a conducting channel layer. The specific contact resistance (ρ_C) at the source or drain contact decreases as the gate voltage is increased from 0 to 10 V. The devices fabricated with Ni S/D electrodes show the best TFT characteristics such as highest field effect mobility (16.09 $cm^2/V\cdot s$), ON/OFF current ratio (3.27×10^6), lowest sub-threshold slope (0.10 V/dec) and specific contact resistance (8.62 $\Omega\cdot cm^2$ at V_G=0 V). This is found that the interfacial reaction between Al and a-ITZO semiconducting layer lead to the negative shift of threshold voltage. There is a trend that the specific contact resistance decreases with increasing the work function of S/D electrode. This result can be partially ascribed to better band alignment in the Ni/ITZO interface due to the work function of Ni (5.04–5.35 eV) and ITZO (5.00–6.10 eV) being somewhat similar.

1. Introduction

Recently, thin film transistors (TFTs) based on amorphous oxide semiconductors (AOSs) have been used for electronic applications, such as touch panels, active-matrix flat panel displays, and active-matrix organic light-emitting diode (AMOLED) displays, due to the improvement when compared with conventional amorphous and polycrystalline silicon based devices [1–3]. In particular, amorphous indium tin zinc oxide (a-ITZO) is a promising AOS candidate material with high mobility (>10 $cm^2/V\cdot s$) [4], high transparency ($>85\%$) in the visible range [5], and good uniform surface planarity [6] even the film is deposited at room temperature.

Specific contact resistance (ρ_C) is defined as the resistance presented to uniform current flow across the interface of unit area between the metallization and semiconductor layers. However, the contact properties between source/drain (S/D) electrodes and the a-ITZO channel layer at different channel lengths have not been reported. The accurate understanding

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of these properties is important, because a high contact resistance in S/D contacts is the major cause of current crowding, wherein accumulated electron flows directly impact the electrical properties of TFTs, such as threshold voltage (V_{TH}), field effect mobility (μ_{FE}), ON/OFF current ratio (I_{ON}/I_{OFF}), and subthreshold swing (SS).

The a-ITZO is a natural n-type semiconductor. This is observed that In-5s and Sn-5s meet the electronic configuration $(n-1)d^{10}ns^0$ $(n \geq 5)$ of heavy post-transition metal cation for AOS [3]. The conduction band minimum states of a-ITZO are found to consist mainly of the In-5s and Sn-5s atomic orbital states [7]. The In-5s and Sn-5s cations make similar contributions to form the electron conduction in the a-ITZO. Thus, the electron is the dominant carrier in the ITZO bulk. As Sunghwan Lee et al. [8] reported, the low carrier concentration in the TFT channel improve the performance of transistors. The improved specific contact resistance was acquired with a high carrier density which is not suitable for TFT channel material. Otherwise, when the contact resistance is large, a high applied bias is needed across the S/D to inject carriers into the device, resulting in low reported mobility. Furthermore, due to the high work function (4.9–6.1 eV) [9], and high carrier concentration of a-ITZO film, this is significant to find the S/D material to create low ρ_C on the contact between S/D electrodes and active layer.

The investigation described in this manuscript focuses on the influence of ρ_C on the interface between a-ITZO channel layer and S/D electrodes, and their effects on electrical characteristics of a-ITZO based TFTs to provide better performance. The degradation in the TFT performance of short channel structures owing to the contact resistance is also discussed. These resistances were extracted by the well-known transmission line method (TLM) with different channel lengths and gate voltages (V_G) applied.

2. Experimental

Fig. 1(a) shows the schematic cross-section view of the staggered bottom-gate structure ITZO–TFT. Commercially available SiO_2 coated *p*-type-crystalline silicon substrates (SiO_2 acting as the common gate insulator) were placed. These substrates were cleaned with acetone, iso-propyl-alcohol and de-ionized water in an ultrasonic bath for 10 min. The ITZO active channel was 50 nm thick and deposited by DC magnetron sputtering using a ceramic ITZO target (In_2O_3: SnO_2: ZnO=30:35:35 at. %) at room temperature. The DC power and working pressure were maintained at 80 W and 5 m Torr, respectively. The ratio of Ar and O_2 gas flow rates were Ar/O_2=14/6. After the deposition, the samples were annealed using rapid thermal annealing (RTA) equipment at 350 °C for one hour under oxygen ambience in the furnace. The S/D electrodes were formed with 150 nm thickness. Al and Ni electrodes were deposited by thermal evaporation. The ITO electrode was deposited by DC sputtering system at 100 W, and 5 m Torr. For the investigation of specific contact resistance, TLM patterns consisting of a fixed channel width (W) of 1600 μm and lengths (L) ranging from 200 (short channel) to 800 μm (long channel) at 200 μm steps were formed in the same channel region (Fig. 1(a)). So the W/L ratios were 8/1, 4/1, 8/3, and 2/1, respectively. These structures offer a range of channel lengths to allow the extraction of channel resistivity and channel/metallization specific contact resistance via the TLM method [8,10]. The electrical performance of the TFT devices was characterized using an EL 420 C semiconductor parameter analyzer. All the measurements were carried out at room temperature in the dark.

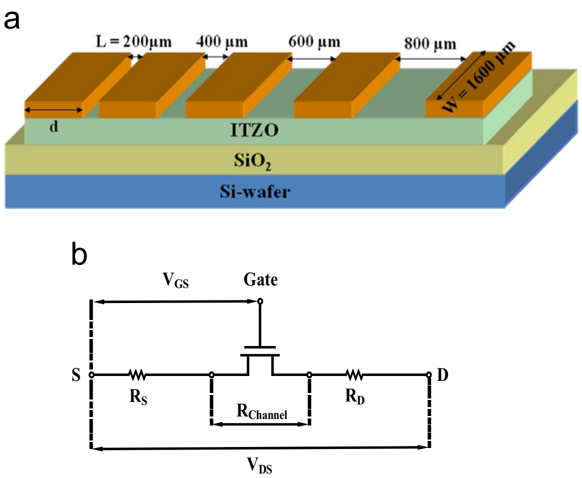

Fig. 1. (a) Schematic diagram of TLM patterns in ITZO TFTs and (b) an equivalent circuit model for TFTs.

3. Results and discussions

Fig. 1(b) shows the schematic diagram of TLM patterns in ITZO TFTs. The total resistance (R_{Total}) measured in each of the TLM configurations is a function of the contact resistance at the two channel/contact interfaces and the sheet resistance of the channel [8,11]:

$$R_{Total} = 2R_C + R_{ch} \tag{1}$$

with

$$R_{ch} = \frac{R_S}{W} L \tag{2}$$

where R_C is the contact resistance between channel and S/D electrodes, R_S is the sheet resistance of the semiconducting layer outside the contact, and R_{ch} is the channel resistance.

The relationship between contact resistance R_C and ρ_C is given by [10]

$$R_C = \frac{1}{W}\sqrt{R_S \rho_C}\coth\left(\sqrt{\frac{R_S}{\rho_C}}d\right) \approx \frac{1}{W}\sqrt{R_S \rho_C} \approx \frac{\rho_C}{W L_T} \tag{3}$$

$$L_T = \left(\frac{\rho_C}{R_S}\right)^{1/2} \tag{4}$$

where d is the contact length and L_T is the transfer length, which is the effective length of the S/D electrodes.

Fig. 2 presents the transfer characteristics of ITZO–TFTs with Al S/D contacts at drain voltage V_D=1 V. The V_G is swept from −15 to 15 V. The threshold voltage of the TFTs increases with increasing L. The samples with the W/L