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A novel LDMOS structure using P-trench for high performance applications

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ABSTRACT

In this paper, we propose a new structure of silicon on insulator (SOI) lateral diffused metal oxide semiconductor (LDMOS) field effect transistors to improve the device performance. In the proposed structure, a trench is created in the buried oxide under the drift and drain regions and filled with p-type Si. We called the proposed structure as P-trench SOI-LDMOS (PT-LDMOS). Our simulations with two dimensional ATLAS simulator shows the unique features exhibited by the proposed structure in comparison with a conventional SOI-LDMOS (C-LDMOS). In the PT-LDMOS, the electric field is modified by producing a new additional peak at the electric field distribution, reducing the magnitude of electric field peak near the gate edge, removing of electric field crowding near the drift and drain junction at the bottom surface of the silicon layer, and making the surface electric field distribution more smooth. We optimize the doping concentration and the dimensions of the P-trench in the PT-LDMOS structure. Hence, the results illustrate the benefits of high performance PT-LDMOS over conventional one and expand the application of SOI-LDMOSs to high voltage.

1. Introduction

Due to the significant advantages of lateral double diffused MOSFET (LDMOS) structure compared to traditional structures including, high compatibility for integration into modern BiCMOS power technologies, high power gain and efficiency, and low cost, this structure has been extensively utilized in intelligent power integrated circuits [1–4].

On the other hand, by considering the numerous benefits that is provided by silicon on insulator (SOI) technology such as ideal dielectric isolation, compactness, high speed, high temperature capability, and low loss, there is a great interest in applying these structures for production of high-voltage lateral devices [5–8].

In SOI structure for power devices due to the existence of buried oxide layer, two issues have attracted the attention of self-heating effect (SHE) and low breakdown voltage [9–11]. In recent years, numerous schemes have been proposed for SOI-LDMOS to improve the performance of the device and solve these problems [12–14].

In this paper a new structure is presented for LDMOS devices to overcome the low breakdown voltage problem. The proposed structure enhances the breakdown voltage by applying a P-trench that is placed under the drift and drain regions. We called the proposed structure as P-trench SOI-LDMOS (PT-LDMOS). In this work, it will be illustrated that the electric field of the proposed structure is modified by producing an additional electric field peak, reducing the peak of electric field near the gate edge, and removing the electric field crowding near the drift and drain junction at the bottom surface of the silicon layer. Therefore, access to a more homogenous curve for the electric field distribution will be available in the PT-LDMOS structure and the

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characteristics of conventional SOI-LDMOS (C-LDMOS) are significantly improved. So, first the proposed structure will be introduced and then we will present two-dimensional numerical simulation results [15] of the proposed structure and the influence of the P-trench will be compared with the C-LDMOS characteristics.

2. Device structure and simulation method

Fig. 1 shows the schematic cross-sectional view of the proposed structure. As shown in the figure, a trench is created in the buried oxide at the drain side and filled with p-type doping to improve the breakdown voltage. The physical parameters used for simulating the PT-LDMOS structure are equivalent to the device parameters of the C-LDMOS structure, but the C-LDMOS structure does not have the P-trench in the buried oxide. These values are specified in Table 1. Also the width of the device for both the structures is 1 μm.

In order to investigate the effects of P-trench creating at PT-LDMOS performance the simulations carried out by using ATLAS 2-D device simulator. Various models including, "SRH", "Auger", "Analytic", "Fldmob", "Incomplete", and "Impact Selb"are utilized in simulation to reach more actual results.

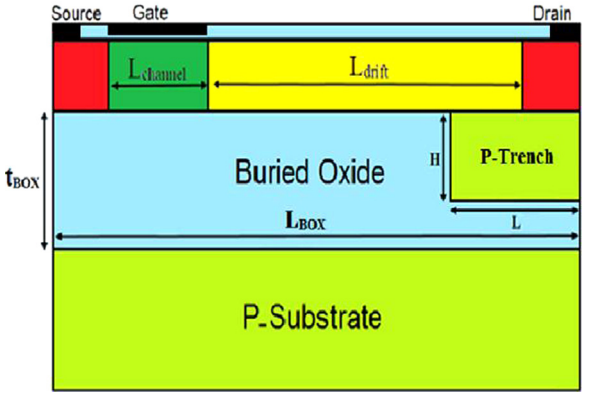

Fig. 1. Cross section of the PT-LDMOS structure.

Table 1
Device simulation parameters.

Parameters	Symbol	Value	Unit
Length of drift region	L_{drift}	10	μm
Length of buried oxide	L_{BOX}	14	μm
Thickness of buried oxide	t_{BOX}	1	μm
Height of P-trench	H	0.9	μm
Length of P-trench	L	4	μm
Doping of P-trench	N_t	1×10^{13}	cm^{-3}
N^+ Source/drain doping	N_n	1×10^{19}	cm^{-3}
Doping of N^- drift region	N_d	2×10^{16}	cm^{-3}
Doping of P-substrate layer	N_{sub}	1×10^{13}	cm^{-3}
Length of channel	$L_{channel}$	2	μm

3. Discussion and results

When the applied voltage between the drain and source for the C-LDMOS structure is equal to breakdown voltage, the height of the electrical field peaks is close to a critical amount at two regions; one at the gate edge side to drift region at the top surface of the silicon layer and the other one is placed near the drift and drain junction region at the bottom surface of the silicon layer [16] as illustrated in Fig. 2. The figure shows the 2-D electric field curves at the top surface and the bottom surface of the silicon layer for the C-LDMOS and PT-LDMOS structures, respectively. So, the high breakdown voltage can be provided by reducing the electric field peak in these regions. The P-trench that is used in the proposed structure leads to the displacement of electric field crowding near the drift/drain junction at the bottom surface of the silicon layer and putting it at the bottom surface of P-trench in the buried oxide, creating an additional peak at the electric field distribution, reducing the peak of electric field near the gate edge, modifying the electric field in the drift region and monotonous surface electric field distribution. Therefore, it is possible to achieve higher breakdown voltage (V_{BR}) in the proposed structure

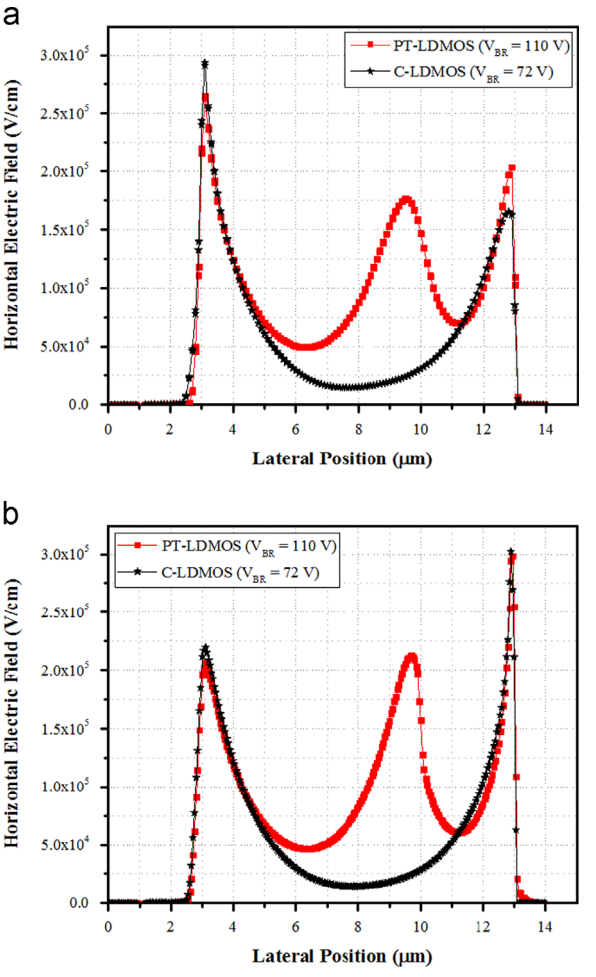

Fig. 2. Electric field distribution for the C-LDMOS and PT-LDMOS structures at (a) top surface and (b) bottom surface of the silicon layer.