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All-optical XOR, NOR, and NAND logic functions with parallel semiconductor optical amplifier-based Mach-Zehnder interferometer modules

Amer Kotb [a,b,*], Kyriakos E. Zoiros [c], Chunlei Guo [a,d,*]

[a] The Guo China-US Photonics Laboratory, Changchun Institute of Optics, Fine Mechanics, and Physics, Chinese Academy of Sciences, Changchun 130033, China
[b] Department of Physics, Faculty of Science, University of Fayoum, Fayoum 63514, Egypt
[c] Lightwave Communications Research Group, Department of Electrical and Computer Engineering, School of Engineering, Democritus University of Thrace, Xanthi 67100, Greece
[d] The Institute of Optics, University of Rochester, Rochester, NY 14627, USA

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ABSTRACT

The performance of XOR, NOR, and NAND functions implemented all-optically (AO) using two parallel semiconductor optical amplifier (SOA)-based Mach-Zehnder interferometers is simulated and investigated. The dependence of the quality factor on key input signals and SOAs parameters is investigated and assessed. The obtained results show that the target AO Boolean functions can simultaneously be realized with the employed scheme with both logical correctness and high quality at 80 Gb/s.

1. Introduction

A key requirement in the effort to manipulate information at a fundamental and system-oriented level entirely in the optical domain, i.e. all-optically (AO), and hence avoid cumbersome optical-to-electrical-to-optical conversions is the ability to execute Boolean functions exclusively by means of light between data modulated signals at ultrafast line rates [1]. Among these functions, the XOR, NOR, and NAND are particularly distinguished due to the special role that they play in the design and realization of AO circuits and subsystems of enhanced logic functionality. More specifically, the XOR function is decisively involved in indispensable AO digital processing [2] and arithmetic [3] tasks. The NOR and the NAND are universal functions by repeated use of which it is possible to synthesize any Boolean function and hence construct any digital circuit [4]. Among various technological approaches that have been proposed for the AO implementation of these core Boolean functions, those that rely on semiconductor optical amplifiers (SOA) have been widely adopted [5] owing to these devices' attractive features of signal amplification, similar to other existing alternatives [6], wide gain bandwidth, strong nonlinearity, reasonable switching energy, low power consumption, compact structure, and proven integration potential. At the same time, it is desirable from a practical perspective to perform all these three functions simultaneously without changing each time the switching module and the way it is configured or driven, so as to enable flexible, smart, reliable and repeatable operation, optimum use of hardware resources, reduced cost and complexity, formation of programmable gate units and arrays, construction of large multi-port switch fabrics as well as of multistage architectures and advanced degree of transparency and intelligence at the optical layer [7]. The achievement of this reconfigurability has been pursued based on SOAs either alone, in conjunction with optical filters, or by incorporating them in an interferometric arrangement. More specifically, in the first case [8], the cross-gain modulation (XGM) effect is exploited in multiple SOA replicas, which are suitably interconnected to obtain the AO XOR, NAND and NOR logic functions. However, XGM suffers from high induced chirp and relatively low output contrast ratio, which deteriorates the quality of the logical outcome, especially when the latter must be combined with another one obtained in a similar fashion. In the second case [9], several carefully detuned filters of identical passband shape, slope, and width are concurrently employed at the

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* Corresponding authors at: The Guo China-US Photonics Laboratory, Changchun Institute of Optics, Fine Mechanics, and Physics, Chinese Academy of Sciences, Changchun 130033, China.

E-mail addresses: amer@ciomp.ac.cn (A. Kotb), guo@optics.rochester.edu (C. Guo).

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outputs of an equal number of SOAs to selectively pass or eliminate spectrally broadened portions of the signal to be switched. This method, however, suffers from lack of versatility, especially when it must be adapted to combinational or sequential applications [10]. Additionally, issues such as pulse format preservation and decreased optical signal-to-noise ratio due to the suppression not only of the target spectral components according to the principle exploited for AO logic but also of useful information compromise the scheme' global usability. Finally, in the third case, SOAs are placed in the Mach-Zehnder Interferometer (MZI) to form the building block, which constitutes by far the primary choice for AO switching purposes [11]. However, the desired logic functions are obtained by cascading extra switching stages or launching into a SOA the pair of strong data streams, which comes at the expense of increased complexity, latency, and footprint and heavy strain on the SOA gain dynamics with undesirable consequences for the overall performance and feasibility of the respective schemes [12,13]. An alternative option, which has been proposed to simultaneously execute the considered logic functions, uses two SOA-based MZI structures in parallel [14]. This topology provides more freedom and autonomy in handling, adjusting, controlling, and optimizing the relevant setup, which requires less hardware than its conventional counterparts having the same aim [15,16]. Moreover, by simultaneously executing dual target logic functions, the operation of each one of these functions becomes independent of the other, thus making the task of their performance improvement more versatile and efficient. Concurrently, it allows for latency reduction, more affordable driving switching energy and blocking of interstage pattern effect accumulation encountered in cascaded interconnection architectures, as well as information processing in a pipeline fashion with better fanout capability. In this manner, it can better satisfy the key requirements for efficiently implementing AO ultrafast digital circuits and subsystems of enhanced functionality. Thus, in this paper, we follow this idea and extend its applicability it in two ways: First, by extending the AO logic functions speed of operation at 80 Gb/s, which compared to [14] corresponds to an eight-fold increase so as to comply with the trends of single-channel data rates in modern lightwave networks. Second, by demonstrating that these Boolean functionalities can also be executed between pulses of return-to-zero (RZ) data format, which, unlike the non-RZ ones used in [14], exhibits superior transmission properties [17]. For this purpose, we conduct an extensive theoretical treatment based on numerical simulation to study the performance of the AO XOR, NOR, and NAND functions. This is done by employing as metric the quality factor (QF), which, by definition [18], characterizes the logic operation across the entire switched data and hence is more rigorous than when only two extreme binary values are taken into account, as in [14]. The impact of key input signals and SOAs operating parameters is investigated and assessed for each function. In order to obtain reasonable results, the effects of the amplified spontaneous emission (ASE) and the operating temperature on the QF are also taken into account in the simulations. The obtained results show that the target AO functions can simultaneously be executed with both logical correctness and high quality at the pursued data rate.

2. Gates' implementation

2.1. Operation principle

In the proposed design shown in Fig. 1, a continuous wave (CW) signal acting as the 'probe' is repeatedly split and launched into each arm of two parallel MZIs. Concurrently, the data signals (A and B) between which it is intended to execute the target AO logic functions are launched into the two MZIs acting as the 'pumps'.

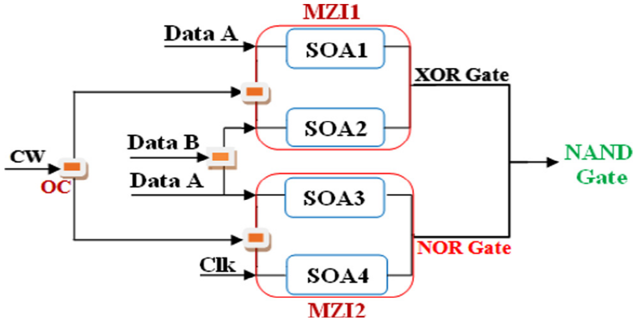

Fig. 1. Schematic of two-parallel SOA-MZIs-based all-optical XOR, NOR, and NAND gates. OC: 3 dB optical coupler.

MZI1 is used in order to realize the XOR gate. Data A and B induce a phase shift on the CW beam via the cross-phase modulation (XPM) effect. When both A and B are '0', MZI1 remains balanced and the logic outcome is '0'. When A = '1' and B = '0', the CW beam constituents in MZI1 upper and lower arms undergo phase changes via XPM. Thus, when they recombine at exit point '9' they interfere constructively and the output is '1'. The same result is obtained when A = '0' and B = '1'. However, when both A and B are '1', the CW beams experience identical phase changes, so they interfere destructively and the output is '0'. In this manner, the XOR gate is obtained.

For NOR operation, the incoming data (A and B) and the clock signals are launched into the upper and lower arms of the lower MZI, respectively. The data and the clock signals are capable of incurring the same gain and phase modulation in each MZI2 arm. When signals A and B are (01, 10 or 11) and the clock signal is all 1's, the MZI2 becomes more saturated, therefore the probe signal travelling through the two arms will be either (10, 01 or 11), which upon destructive interference results in '0' at the output. On the other hand, when both A and B are '0', the clock signal will break the phase balance of MZI2 and constructive interference occurs at the output of MZI2, which results in logic '1'. In this manner, the Boolean NOR gate is achieved. Then the logic outcomes of the XOR and the NOR gates are combined to realize, by definition, the NAND operation.

2.2. Simulation

The SOA-MZIs time-dependent response is described by the following first-order coupled differential equations [19,20]:

$$\frac{dh_{CD}(t)}{dt} = \frac{h_0 - h_{CD}(t)}{\tau_C} - (exp[h_{CD}(t) + h_{CH}(t) + h_{SHB}(t)] - 1)\frac{P_{in}(t)}{E_{sat}} \tag{1}$$

$$\frac{dh_{CH}(t)}{dt} = -\frac{h_{CH}(t)}{\tau_{CH}} - \frac{\varepsilon_{CH}}{\tau_{CH}}(\,exp\,[h_{CD}\,(t) + h_{CH}(t) + h_{SHB}(t)] - 1)\,P_{in}(t) \tag{2}$$

$$\frac{dh_{SHB}(t)}{dt} = -\frac{h_{SHB}(t)}{\tau_{SHB}} - \frac{\varepsilon_{SHB}}{\tau_{SHB}}(\,exp\,[h_{CD}\,(t) + h_{CH}(t) + h_{SHB}(t)] - 1)\,P_{in}(t) - \frac{dh_{CD}(t)}{dt} - \frac{dh_{CH}(t)}{dt} \tag{3}$$

where the SOA's gains integrated over the active region length, $h_{CD}(t)$, $h_{CH}(t)$, and $h_{SHB}(t)$, are induced by interband effects, which include the carrier depletion (CD), and intraband effects, which include carrier heating (CH) and spectral hole burning (SHB). $h_0 = \ln[G_0]$, where G_0 is the unsaturated power gain. $P_{in}(t)$ is the total