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Optical logic gates using binary decision diagram with mirrors

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Optical circuits of different logical operations using binary decision diagram (BDD) are proposed and described in this paper. A simple table-top model using plane mirrors based on this architecture has been shown in this manuscript. This model is the macroscopic form of micro-electromechanical (MEMS) optical switch, which is also described in this manuscript. Numerical simulations using torsion type micromirrors have been done to find its operational performance. The design is simple and easy to implement for higher bit also.

1. Introduction

Modern computers are based on electronics. If we replace electrons with photons then several advantages such as low crosstalk, high speed and bandwidth, parallel signal processing can be possible. Hence optical switching and interconnections will be the best alternative for the coming generation supercomputing [1–5]. Also two important aspects of all-optical computing are the possibility to integrate a large number of devices in a small chip and the possibility to cascade a large number of devices. Logic gates are the gateway to construct complex computational circuits. Optimization of a logic circuit is an important factor because small number of circuit components and complexity makes a circuit low power consuming and compact in size. In optoelectronic circuit optical to electrical to optical (O–E–O) conversion should be avoided because it decreases the switching speed. Recently non-linear all-optical switching based on fiber Bragg grating has been reported due to their low threshold power and low insertion loss [6–8]. Also nonlinear material based interferometric switches make revolution in all-optical switching [9–15]. But the control signals of these interferometric switches are of high intensity, which consume high power. We can avoid power consumption in the circuit by a trick which was shown by Hardy and Shamir in their paper [16]. They showed that control signals should not have the logic symbol to the later cell i.e. control signal outputs can not be reused to the internal circuit. Then we have to require optical attenuator to decrease its intensity, which generates heat. Also vice versa should be avoided. For this operation optical power should have to increase by optical amplifier, which increases power consumption. Hence control signal and data signal cannot be mixed up. In optical computation optical data should follow a path according to the selection of control. A data that enters into the circuit must come to the output i.e. data must be conserved. All these criteria can be well utilized by binary decision diagram (BDD) architecture. Hence it will play a significant role in high speed and low power optical circuits in future supercomputing. BDDs were first introduced by Akers [17] and further improved by Bryant [18]. BDD is a graphical way to represent a function and also an alternative circuit optimization technique like well known Karnaugh maps and algebraic manipulation [18,19]. Also BDD based optimization techniques are successfully used in communication system [20].

In electronics BDD many circuits have been proposed and experimentally verified. Such as, Yano et al. [21] designed BDD based pass transistor logic circuits. Asahi et al. [22] demonstrated BDD circuits by single electron devices. Biswas and Sarkar [23] also designed an arithmetic logic unit BDD architecture based on single electron transport system.

Many proposals have also been made in quantum circuits. Such as, Yoshikawa et al. designed rapid single flux quantum (RSFQ) logic circuits [24] and 1-bit microprocessor [25] based on BDD. Zhao et al. fabricated BDD based two bit arithmetic logic unit [26] and AND-OR logic units [27] by GaAs-nanoware quantum hexagonal topology.

But in optical computing only one approach is taken so far. Lin et al. [28] demonstrated optical binary decision diagram based two bit adder using ring resonator in their recent paper. They use three different wavelengths of light in their circuits.

In my proposal Boolean logical operations (16-logic functions) with BDD architecture has been proposed and described. This architecture can be easily designed using plane mirrors. Mirrors are linear passive optical components. No amplification of light or

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interference happens here. It only reflects light. So it is very simple. The basic technique of this mirror based BDD design is that we have to arrange the mirrors in a special design such that we can do computing with it without any hazard and difficulty. A simple table-top model of two variable BDD based XOR/AND logic circuit with mirrors is shown. Logic circuit with the table top model is very easy to design. We can get all of the 16-logic operations from a single circuit which is the major advantage of the proposed scheme. There is no active component used in this design, only passive optical components (plane mirrors) are used in this circuit. Hence the circuit is low cost and very easy to understand. The possibility of this proposed circuit in chip level using micro-electromechanical (MEMS) optical switches is also discussed in this manuscript. Complex logic operation can be possible using this design with addition of more mirrors.

2. Binary decision diagram (BDD)

Binary decision diagram (BDD) is a reduced form of a binary decision tree (BDT) [29]. All-optical BDT structure design has already been proposed in our previous literature [30,31]. Any Boolean function $f: B^n \rightarrow B$ can be represented by BDD (where n is the number of variables) [18]. According to “Shannon decomposition” the function f can be decomposed in terms of variable ‘x’ as follows:

$$f = (\neg x_i f_{x_i=0} + x_i f_{x_i=1}), \quad (1 \le i \le n) \tag{1}$$

The functions $f_{x_i=0}$ and $f_{x_i=1}$ are the cofactors of the function f. In the following, the node representing $f_{x_i=0}$ ($f_{x_i=1}$) is denoted by *low*(*node*) (*high*(*node*)), while x_i ($\neg x_i$) is called the select variable (and its inverse) [32]. The one input terminal node is called ‘root’. The logical representation of node in BDD architecture is shown in Fig. 1(a). In practical the node can be designed by a mirror (M) in optical implementation, which is shown in Fig. 1(b). The presence and absence of the mirror is considered the select variable x_i and $\neg x_i$ respectively. Light coming from ‘S’ is reflected toward ‘H’ if the mirror is present (i.e. $x_i = 1$or high) or towards ‘L’ if mirror is absent (i.e. $x_i = 0$ or $\neg x_i$ or low). We can design BDD architecture by mirrors, which is discussed in the next section.

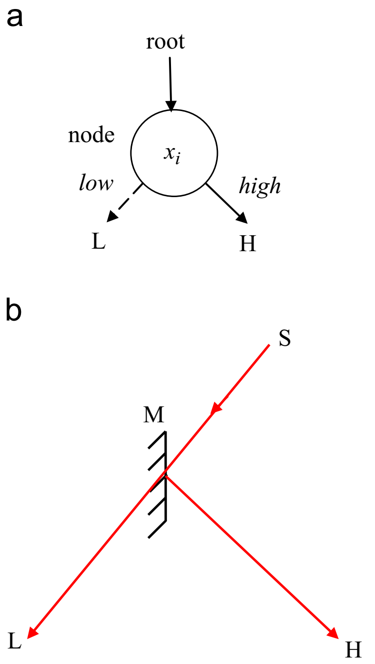

Fig. 1. (a). Logical representation of node in BDD If $x_i = 1$ the decision is ‘*high*’ (*H*) and for $x_i = 0$ the decision is ‘*low*’ (*L*). (b): Optical representation of a node by mirror (*M* or comb like symbol). The presence and absence of the mirror is considered the select variable. Light comes from ‘*S*’ is reflected toward ‘*H*’ if the mirror is present or towards ‘*L*’ if mirror is absent.

3. Optical binary logic circuits by BDD with mirrors (table top design)

Binary logic (radix=2) has two logical states ‘0’ and ‘1’. Depending on the number of variables (n) used, different logic functions can be generated. The number of possible functions (N) in binary logic can be expressed as.

$$N = 2^{(2^n)} \tag{2}$$

In two variables ($n = 2$) binary logic, there are $2^{2^2} = 16$ functions that can be possible [33,34]. The BDD of these logical functions is shown in Table 1. Mirrors can be placed in every node of the BDD architecture, which is written from the previous section. Hence optical circuit of these logical operations can be easily designed using plane mirrors.

As an example, two logical functions $f_1 = (A \oplus B)$ and $f_2 = A \wedge B$ can be easily designed with mirrors in a single circuit, which is shown in Fig. 2. Here f_1 is ‘ANTIVALENCE’ or ‘XOR’ operation and f_2 is ‘CONJUNCTION’ or ‘AND’ operation. ‘S’ is a light source (in model, I use laser torch as optical source). Four mirrors construct the circuit. One-‘A’, two-‘B’ mirrors and other is a fixed mirror (FM). ‘A’ and ‘B’ mirrors are movable i.e. select variables (A and B) can be applied by these mirrors. It is a two variables circuit. This combined circuit is well known as ‘1-bit adder’. For optical outputs logic-‘1’ and logic-‘0’ are indicated by ‘presence of light’ and ‘no light’ respectively. For mirror control operation logic-‘1’ and logic-‘0’ are indicated by ‘presences’ and ‘absence’ of mirror respectively. The operation of this circuit is discussed below.

Case-I (A=B=0): When mirrors marked with ‘A’ and ‘B’ are absent then light goes straight from source (S), as shown in Fig. 3(a)-(i). No light is found at D1 and D2 screen. This result is obtained from the photograph (Fig. 3(a)-(ii)) also. That is for $A=B=0$ the outputs are D1=D2=0.

Case-II (A=0, B=1): When mirrors marked with ‘A’ is absent but ‘B’ mirrors are present, then light from S follows the path indicated by Fig. 3(b)-(i) and reaches to the screen D1. No light reaches at D2 screen. In photograph (Fig. 3(b)-(ii)) we can see a light spot at screen D1 only. That is for $A=0$, $B=1$ the outputs D1=1 and D2=0 respectively.

Case-III (A=1, B=0): When mirrors marked with ‘A’ is present but ‘B’s are absent, then light from S follows the path indicated by Fig. 3(c)-(i) and reaches to the screen D1 again. No light reaches at D2 screen. In photograph (Fig. 3(c)-(ii)) we can see a light spot on screen D1 only. That is for $A=1$, $B=0$ the outputs D1=1 and D2=0 respectively.

Case-IV (A=B=1): When mirrors marked with ‘A’ and ‘B’ are both present, then light from S follows the path indicated by Fig. 3(d)-(i) and reaches to the screen D2. No light reaches at D1 screen. In photograph (Fig. 3(d)-(ii)) we can see a light spot on screen D2 only. That is for $A=B=1$ the outputs are D1=0 and D2=1.

‘Table top’ design is very easy to implement because the operation is straightforward. Here the operations have been done by ‘placing’ and ‘removing’ the mirrors by human effort. We get the results from look up table (LUT). LUT can be written by just viewing the outputs at the screens D1and D2 shown on Table 2(a). From this LUT we can write truth table of the two logical functions $f_1 = (A \oplus B)$ and $f_2 = A \wedge B$ (shown in Table 2(b)). The difficulty of this