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A high stability and uniformity W micro hot plate

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ABSTRACT

In this paper, we report on the simulation, design, fabrication and characterization of a tungsten (W) hot plate with a high electro-thermal stability and thermal uniform distribution. The device is constituted by a tungsten multi-rings resistor embedded in a dielectric membrane. Different layouts have been simulated, drawn and tested in order to evaluate and optimize the uniformity of the hot region and the power consumption. For the optimized device the diameter of the hot plate region is 1.25 mm, instead the membrane diameter is 1.83 mm. An innovative layout has been drawn to monitor the temperature uniformity of the hot region: distributed contacts have been integrated on it to be used as sense terminals and to extrapolate the single ring temperature. The same W resistor branches are used as thermal sensors by evaluating in advance the TCR (Temperature Coefficient of Resistance) and extrapolating the temperature by the resistance change. Thermal mapping shows that the temperature uniformity over the heated area is lower than 6% at 400 °C with a power consumption of only 135 mW.

Thermal treatments have been performed in order to enhance the device thermal and electrical performances repeatability on wafer.

1. Introduction

The applications of MEMS micro-hot-plates is rapidly growing for infrared emitters [1,2], gas sensors [3,4], and thermal actuators, Pirani gas pressure sensor [5], biological sensors [6] etc... For such applications the devices require low power consumption, thermal uniformity, stability and robustness. Usually the hot plate is formed by a heater embedded in a released membrane, thermally isolated by the silicon substrate to reduce the thermal dispersion and achieve very high temperatures. When the electrical current flows in the heater, the temperature in the active region increases, producing also emission in the infrared range. Micro-hot-plates have been fabricated using different materials, such as, platinum [2,7] or polysilicon heaters [8] embedded within a membrane consisting of silicon dioxide or silicon nitride or multi-stack to compensate the tensile and compressive stress of the single layer.

However, the use of platinum is not compatible with CMOS processes and devices based on doped polysilicon are known to suffer from long-term stability problems at high temperatures (over 300 °C) [8]

W heaters have been integrated in order to be full CMOS compatible, low cost, robust and highly reproducible. Moreover the W melting temperature is 3422 °C and this could expand the working temperature up limit [9,10].

In this work we report on the simulation, design, fabrication and characterization of a tungsten multi-rings heater embedded in a released dielectric membrane to be used as infrared source. To use the hot plate as an infrared source it's necessary to enlarge the heater dimensions to increase the emitted power. In this case the power consumption, the thermal uniformity and the mechanical-thermal stress are crucial specifications [11]. In despite of the large dimension (circular heater diameter = 1.25 mm) the hot plate described in this paper presents a uniform thermal distribution also at high temperatures. The hot plate design is optimized to be used as IR emitter within an NDIR sensor, thanks to the large area, and for this reason 400 °C has been selected as operating temperature to achieve infrared emission peaked at 4.3um [12]. Different layouts have been simulated, drawn and tested in order to evaluate the uniformity of the hot region. To monitor the active region temperature, an innovative layout has been conceived: distributed contacts have been integrated on the heater to divide it into sectors, used as temperature sensors exploiting their own resistance variation with temperature to extrapolate the thermal distribution. The data show that the percentage thermal variation on active area increases at higher temperatures: the temperature uniformity over the heated

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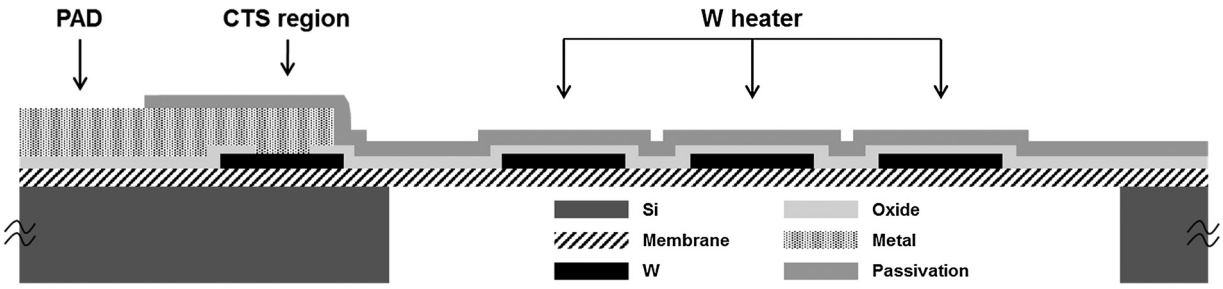

Fig. 1. Schematic cross-section of the device.

area ranges from 1% at 135 °C up to 7% at 560 °C for the optimized device. The thermal uniformity data have been compared with the device thermal map acquired with an infrared optical microscope: the results using the two different methods are strictly in accord, validating the implemented electrical one.

By increasing the membrane edge and reducing the SiN passivation thickness, the power consumption has been minimized to only 135 mW for a temperature of 400 °C.

Thermal treatments ranging from 600° to 800 °C have been performed in order to enhance the process stability and, then, the device electrical performances repeatability on wafer: the devices have been tested before and after a stress test at 530 °C for 120 h.

The process flow is entirely compatible with CMOS technology and the devices have been fabricated on 8 inch wafer achieving an excellent reproducibility from device-to-device on wafer.

2. Device simulation design and fabrication

The schematic cross section (not in scale) of the micro-hotplate used for simulations is shown in Fig. 1. The processing was done on 8-inch low conductivity wafers. The device consists of a tungsten heater embedded in dielectric multilayer membrane, released from the substrate by a back etch process that allows a vertical profile. The dielectric membrane under the W heater (which is 0.2 μm thick) is constituted by a $SiO_2/Si_3N_4/SiO_2$ multistack to compensate the final bent. The passivation over the heater is composed as well by a double layer SiO_2/Si_3N_4. Due to the high thermal conductivity, compared to that of the SiO_2 layer, the Si_3N_4 has been thinned to 200 nm in order to reduce the thermal dissipation toward the device edge and then across the silicon substrate. An Aluminium metallization is used to contact the W heater. When an electrical power is supplied to the heater, its temperature increases due to self-heating effect. The simulation are considered in air.

Circular membranes are more mechanically robust than square ones, therefore a multi-rings structure has been simulated. A full 3D model of the device has been developed using COMSOL MultiphysicTM Ver. 5.2 Finite Element Modelling package. The three main thermal dissipation mechanisms have been considered in the simulations: convection, conduction and radiation. The size of the heater has been maintained constant (diameter = 1.25 mm) instead the distance between the heater edge and the silicon substrate (membrane edge) has been changed from 165 μm to 290 μm in order to better thermally insulate the heater and then reduce the losses, maintaining the mechanical robustness. The wafer thickness is 400 μm.

The W tracks width is not constant, but is modulated in order to improve the thermal uniformity, as shown in Fig. 2a, taking into account the higher dissipation of the external ring versus the silicon substrate.

The thermal properties used for the materials are shown in Table 1.

The W thermal conductivity is 177 W/mK at room temperature, but decreases at higher temperatures. This variation has been taken into account during the simulations, instead for other materials the values have been fixed as reported in Table 1 [13,14]. The device surface emissivity has been estimated at 0.4 by preliminary characterization.

The simulation was performed by fixing the base of the silicon substrate at 25°C and applying a voltage at the heater terminals, extracting the current flowing into the heater and the related average temperature. Also the thermal map can be represented as shown in Fig. 2b and the correspondent surface temperature dis-

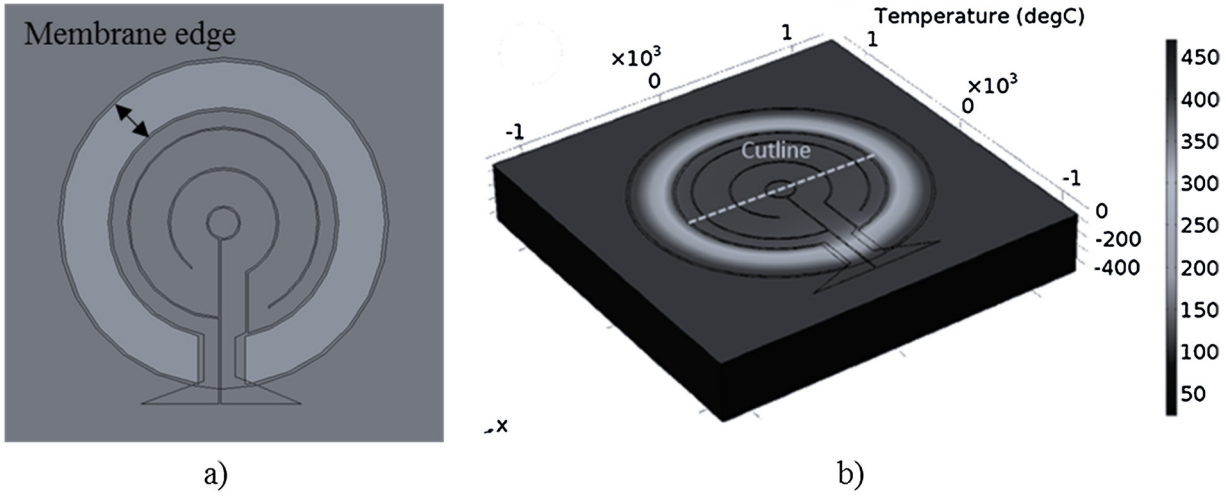

Fig. 2. Schematic layout of the device used for the simulations (a) and example of simulation results in terms of thermal distribution (b).