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A compact, low-power, and fast pulse-width modulation based digital pixel sensor with no bias circuit

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ABSTRACT

A high-speed and compact in-pixel light-to-time converter (LTC), with low power consumption and wide dynamic range is presented. By using the proposed LTC, a digital pixel sensor (DPS) based on a pulse-width modulation (PWM) scheme has been designed and fabricated in a standard 180-nm, single-poly, six-metal complementary metal oxide semiconductor (CMOS) technology. The prototype chip consists of a 16 × 16 pixel array with an individual pixel size of 21 × 21 μm^2 and a fill factor of 39% in the 180-nm CMOS technology. Experimental results show that the circuit operates at supply voltages down to 800 mV and achieves an overall dynamic range of more than 140 dB. The power consumption at 800 mV supply and room light intensity is approximately 2.85 nW.

1. Introduction

CMOS image sensors are currently displacing charge-coupled devices (CCD) in high volume applications where properties such as low cost, low power, low area, and high speed are desired. These sensors are used in various applications, such as digital cameras, robotics, toys, military industrial, space applications, and monitoring systems [1–5]. Most digital cameras are today based on the active pixel sensor (APS), which is referred to as the second-generation CMOS image sensors. A property of this type of sensor is that the voltage swing drops by two transistor threshold voltages ($2V_{tn}$) owing to an nMOS reset transistor and a source follower amplifier [2,5,6]. Thus, as the technology scales the APS output voltage swing will be significantly limited since the supply voltage reduction is faster than that of the threshold voltage [2,7]. Additionally, the signals crossing the pixel array are analog and susceptible to noise coupling via the power lines or the substrate [8]. These factors lead to a poor signal-to-noise ratio (SNR) and low dynamic range [1–8]. Moreover, the output image of an APS sensor suffers from distortion caused by the row-by-row reset and readout operations [9].

Digital pixel sensors, the third generation CMOS image sensors, have been introduced to overcome the weaknesses of the APS structures [3,10]. In the DPS structure, digitization is performed in each pixel and converts the analog signal of the photodetector to a digital value. Most reported in-pixel ADC operation is based on pulse-width modulation [11,12] or pulse-frequency modulation (PFM) techniques [13,14]. The information carried by the analog signal is converted into its equivalent time or frequency information. The performance constraints are transferred from the voltage domain into the time or frequency domain [10]. By this, the DPS offers several benefits over analog sensors, such as: wider dynamic range, because by using modulation techniques, the dynamic range is no longer restricted by the power supply [10]; higher SNR, owing to the close proximity of the ADC to where the signal is generated [2,10]; better scaling with CMOS technology, due to the reduced analog circuit performance demands [2]; and lower fixed-pattern noise (FPN) as a result of the elimination of column FPN and column readout noise [2]. Additionally, in snap shot mode the DPS does not have any image distortion since all pixels operate in parallel [9]. Moreover, the analog readout bottleneck is eliminated, and high-speed digital imaging becomes possible [1,2]. Furthermore, the DPS enables us to build smart image sensors by combining on-chip image acquisition and corresponding signal and image processing [15–17]. The main drawback of the DPS, however, is its large transistor count of each pixel, potentially resulting in a larger pixel size or lower fill factor compared to the analog image sensors [1]. Accordingly, in

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the past few years, much effort has been spent on designing high performance DPSs with a small number of transistors. To achieve this it is essential to design a compact in-pixel ADC with maintained low-power operation and wide dynamic range.

The schematic and timing diagram of a pulse-width modulation based DPS is illustrated in Fig. 1. To initiate a measurement cycle, the photodiode voltage is reset to V_{DD} by applying a pulse to a reset transistor. Subsequently, after opening the reset switch, the photodiode voltage decreases depending on the amount of light intensity. The comparator output changes when the photodiode voltage passes the reference voltage. At this moment, a Gray code available on the data bus, generated by a global counter, is stored into the pixel memory. The stored value, which shows the time between the reset of the photodiode and the change at the comparator output, now determines the light intensity value. The conversion time (T_{conv}) can be calculated as [10]:

$$T_{conv} = \frac{C_{PD}(V_{DD} - V_{ref})}{I_{PD}}, \quad (1)$$

where C_{PD} is the capacitance at the photodiode node, I_{PD} is the photo-generated current along with the dark current, and V_{ref} is the reference voltage. In the pulse-frequency-modulation scheme, the comparator output is fed back to the reset switch, so a pulse train with a frequency proportional to the light intensity is generated at the comparator output. PWM-based DPS are generally preferred over PFM, since they occupy a smaller area and consume less power [10]. These are two key parameters that need to be considered when designing an image sensor.

A 10,000 frame/s imager, which operates based on a PWM scheme is presented in Ref. [18]. All in-pixel ADCs operate in parallel and data read-out is done through a 64-bit wide bus to yield a high-speed imager. Additionally, to decrease conversion time, an analog ramp signal is applied to the reference voltage. Bermak et al. have proposed a PWM DPS based on an asynchronous self-resetting scheme. The conversion time is reconfigurable and its resolution can be adjusted [19]. An asynchronous self-reset scheme is used to avoid a large peak current during the reset phase. A low power PWM-based DPS has been proposed in Ref. [20]. Depending on the photodiode voltage, an additional subthreshold control unit enables or disables the in-pixel ADC. This additional unit does decrease the ADC static power consumption but also decreases the pixel fill-factor too. A low-power dynamic comparator with high precision has been proposed in Ref. [21]. The comparator input-referred offset is reduced by using a cancellation scheme, which samples the offset in the time domain and cancels it with a bulk tuning technique. This scheme does not have an adverse impact on the speed or power consumption of the DPS but occupies a larger area. Zhang et al. have employed multi-reset integration scheme to design an 8-bit pixel using a 4-bit PWM-based DPS [22]. They have used a two-transistor dynamic memory (2T-DRAM) and a selective refresh scheme to improve the pixel fill-factor. A digital imager with an adaptive dynamic range and programmable pixel response has been proposed in Ref. [23]. Here an array-based digital control unit linearizes the pixel response and sets the conversion range. Additionally, an asynchronous self-resetting approach is implemented by using a start integration signal instead of a global reset signal to avoid a large peak current. Wang et al. in Ref. [24] have evaluated two-stage comparators in the weak-inversion region to be able to design a compact, robust, low power, and wide dynamic range comparator. Hansen et al. have employed an advanced version of the Wilkinson-type ADC as an in-pixel converter [25]. This ADC has an offset and gain trimming capability, but the circuit occupies a large area. Cho et al. have used a single inverter as a converter to obtain a low-power and high fill-factor image sensor [26]. A simple offset cancellation scheme is incorporated with the converter to improve the SNR; however, the sensor has a limited speed and dynamic range.

Most recent works employ a circuit similar to that shown in Fig. 1, trying to improve the circuit performance by improving the performance of the comparator block within the circuit. The aim is to design a robust, fast, low-power, and low-area comparator, which has a low-offset and high gain-bandwidth. Despite many attempts, the presented light-to-time converters have some problems such as long integration time in low-light intensity and weakness in detection of high-light intensities [27]. In Fig. 1, the comparator is biased in the weak-inversion region to decrease the power consumption and also to maximize the gain. It, however, reduces the comparator speed, which results in weak detection of high-light illuminations; it still has high power consumption owing to the static bias circuits; and also has the problem of FPN over the array due to variation of bias currents and voltages between distant pixels. Additionally, the FPN is increased because of the gain and offset variations of the comparators themselves. Also the transistors must be designed with a large gate area to minimize mismatch effects in the weak-inversion region.

In this work, to address the above mentioned problems, a compact, fast, and high operating-range pixel-level LTC is presented. The proposed LTC is a simple mixed-mode circuit without any bias reference circuit that operates at a low supply voltage with a low power consumption. The converter overcomes some weaknesses of previously reported LTCs such as: weakness in detecting high-light illuminations, long conversion time at low-light illuminations, and the presence of FPN due to the diversity of supply voltages and bias currents between distant pixels in the array.

The rest of the paper is organized as follows. The proposed pixel-level LTC and DPS structures and the theoretical framework of their operations are presented in Section 2. Also the physical implementation and corresponding simulation results are presented in this section. The experimental and comparison results of the circuit are given in Section 3. Finally, the work is concluded in Section 4.

2. Proposed structures and implementation data

In this section, the proposed digital pixel sensor is presented and the mathematical expressions are extracted. To verify the functionality of the proposed circuit, it is designed and implemented in a 180-nm CMOS technology. The simulation results are provided to validate the extracted theoretical framework.

2.1. The proposed PWM based digital pixel sensor

A pixel-level light-to-time converter using a mixed-signal circuit is proposed. Using this LTC, a DPS, based on pulse-width modulation, is designed. The following subsections present the architecture of the designed DPS, the pixel-level LTC circuit and its operation, the mathematical description of the LTC operation, and finally the employed in-pixel memory.

2.1.1. Digital pixel sensor architecture

Fig. 2 shows the architecture of the designed PWM-based DPS array and also the block diagram of each pixel in the array. As shown in Fig. 2(a), there is a global Gray counter in the architecture, which is synchronously reset with the sensor array. It assigns the data bus value during the conversion time; and the memory of each pixel captures the value of the bus at a specific time, which is related to the light intensity of the pixel. At the end of the conversion time, in the read-out phase, the counter is disconnected from the data bus. The memory contents of all the pixels are read out through the data bus by sequentially addressing the pixels via the decoders. As evident in Fig. 2(b), each pixel is composed of a reset switch, a photodiode, an LTC, and a memory block. The reset switch charges the