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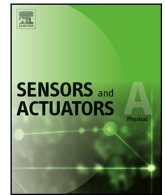

Extremely high-performing heterojunction device by surficial length enhanced effect

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ABSTRACT

High-performing heterojunction devices were achieved by bringing an aluminum-doped ZnO (AZO) into contact with a p-Si substrate. A thin transparent AZO film was directly coated on pillar-array patterned Si and spontaneously formed a rectifying junction without any intentional doping process. Si pillar-arrays were designed to have 5 μm width with variation in periods (7 μm and 10 μm) used to modulate the surficial lengths. The light response is directly proportional to the surficial length enhancement. AZO/Si heterojunction devices showed strong dependence on the incident wavelengths. At a wavelength of 600 nm, the highest response ratio of 70,900% was achieved. We found that the locational superposition of the space charge region and the photo-generated region is crucial for light-reactive responses. We suggest an efficient geometric design scheme for highly efficient light-absorbers.

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1. Introduction

Most photoelectric devices require junction formation. Two-differently doped semiconductor layers in semiconductor devices can establish a p–n junction. A direct contact of metal (M) to a semiconductor (S) spontaneously provides M–S junction or Schottky junction [1]. Similar to the M–S junction, a heterojunction can be achieved from a contact between a semiconducting layer and an extrinsic semiconducting or metallic layer [2].

Transparent conducting oxide (TCO) materials are essential for most photoelectric devices to permit the light transmission of 'in or out' from the light-active junction. Typically, the uses of TCO have been limited for ohmic contacts and thus, have mainly focused on aspects of electrical conductivity, while maintaining a high optical transparency [3]. We previously demonstrated a TCO-semiconductor heterojunction, working as an active rectifying device [4]. This may open a promising opportunity for junction formation without any additional doping process and thus, the processes and fabrication cost would be reduced.

An extended surface is absolutely important for general photoelectric applications, such as photovoltaics, LEDs, and photo-sensors. Various light-active entities have been studied using nanowires, hole-arrays and pillar-arrays [5–8]. A periodic light-absorber has been suggested as being capable of providing a substantially increased optical length [9].

However, little attention has been given to periodic heterojunction devices that use a transparent conductor and semiconductor. Such a design would be an approach that would make it possible to achieve a direct junction device, without a doping process; it would be possible and simultaneously, provide an enormous enlarged light-active region. This design scheme is under consideration as a promising solution for high-performance photoelectric devices that can be produced at a reduced cost.

Herein, we present an extremely high-performing photodetector that operates according to the TCO coating on periodically patterned Si. A transparent conductor of aluminum-doped zinc oxide (AZO) was directly coated on Si pillar-arrays and spontaneously formed a heterojunction, without any additional doping process. Due to its high transparency, the AZO effectively drives the incident light into the Si. Besides, the electrically conductive AZO layer also contributes to the collection of photo-generated carriers.

2. Experimental details

A Czochralski (CZ) grown (1 0 0) p-type Si wafer was used as a substrate; this wafer has resistivity values of 1–10 Ω cm, equivalent to a doping concentration level of around $10^{15}/cm^3$. Pillar structures were fabricated using a photolithography method. Two pillar-structures were designed to have identical width (5 μm) with variations in periods (7 μm and 10 μm) at a fixed depth of 2 μm.

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For heterojunction formation, a transparent conducting layer of AZO was deposited over Si substrates using DC sputtering method with a deposition rate of ~10 nm/min.

The optical transparency of the AZO-film was measured by a UV spectrophotometer (V-570, JASCO) for broad wavelength range (400–1100 nm). An interface layer of the AZO-coated Si was investigated using a field-emission transmission microcopy (TEM, JEOL, JEM-ARM200F). Geometries of Si pillar-arrays were observed by a field emission scanning electron microscopy (SEM, FEI Sirion).

3. Results and discussion

3.1. Fabrication of pillar-arrayed structures

Photolithography was applied to pattern photoresist (PR) masks on the Si substrate, as shown in Fig. 1(a). The PR mask sizes were designed to have 5 μm-size square-shaped arrays with different periodic lengths (7 μm and 10 μm). Negative PR process was performed and subsequently, PR areas were left on the Si substrate after UV-illumination. After this, a reactive ion etching (RIE) step was performed to remove the exposed Si region to a depth of 2 μm. After removing the PR mask patterns, two different pillar-arrays were patterned at a fixed depth of 2 μm. An identical pillar size of 5 μm was formed with variations in periods of 7 μm and 10 μm. These will hereafter be referred to as 5/7 pillar-arrays and 5/10 pillar-arrays. This RIE process is benefit to enhance Si surface, which efficiently increases forward current values. Meanwhile, RIE process also induces Si surface defects and thus causes larger leakage current (Table 1), which will be discussed in a later part.

To make a heterojunction, identical thickness of AZO-coating layers (80 nm) were deposited on different Si substrates of the 5/7 and 5/10 pillar-arrayed patterns. A flat heterojunction device was prepared on a bare Si substrate, for a comparison purpose, using the same AZO deposition process. SEM images are presented for a top-view and a cross-sectional-view of 5/7 pillar-arrays in Fig. 1(b) and (d), respectively. 5/10 pillar-arrays are in Fig. 1(c) and (e), respectively. Fig. 1(f) is an enlarged SEM image, showing a pillar size of 5 μm. Fig. 1(g) was obtained to measure an AZO-coating layer of 80 nm.

3.2. AZO/Si interface analysis and reflectance profiles

The thickness (80 nm) of the AZO film was designed for a quarter wavelength anti-reflection ($d = \lambda/4R$), where R is refractive index of AZO (1.86 at $\lambda = 600$ nm) and λ is wavelength. An AZO film on a flat Si effectively reduces the reflection to 33.44%, with minimum reflection values around 600 nm, as shown in Fig. 2(a). This reflection value is much reduced from the value of 50.79% for bare Si; this reduction is due to the medium refractive index matching of AZO to air of the Si system. For a pillar structure, reflection was substantially suppressed to give 12.5% for the 5/7 pillar-array and 11.38% for the 5/10 pillar-array.

Optical transparency was measured from the 80 nm-thick AZO film coating on a glass substrate. This provides a high transparency of 91.82%, averaged value in the range of 400–1100 nm of wavelengths. Thus, AZO deposition on a Si substrate spontaneously yields a high transparency window. The measured sheet resistance value was as low as 59.10 Ω/□. This optically transparent AZO coating layer works as an antireflection coating layer and an electrically conductive front layer of the AZO/Si heterojunction device.

Fig. 2(b) shows a TEM image of the interface between AZO and Si, projected in the Si [0 1 1] direction. A bottom-inset TEM image clearly shows a single crystalline structure with [1 0 0] orientation of the Si substrate. An AZO film was grown along the [0 0 1] preferential direction on the Si substrate, as shown in the top-inset TEM image. Adjacent lattice spaces in the AZO film are measured to be 0.26 nm, which corresponds to the AZO (0 0 2) plane. This is parallel to the Si (0 0 2) plane, confirming the preferential growth of the AZO film.

A fast Fourier transformation (FFT) of the AZO film was indexed to be Wurtzite ZnO structure. Energy dispersive X-ray spectrometer (EDS) analysis also clearly confirmed the film compositions according to Al, Zn, and O elements, as shown in Fig. 2(c). The AZO-film preferentially grew normal to (0 0 1) basal plane, which has the lowest surface energy in the Wurtzite structure [10]. An amorphous interfacial layer with 2–3 nm thickness was clearly observed between the AZO layer and the Si substrate. Electron energy loss spectroscopy (EELS) analysis was performed in the amorphous interfacial layer (marked as a filled red-circle) and the Si (unfilled black-circle). A strong SiO_2-like Si L (onset 105 eV) energy loss near edge fine structure (ELNES) was detected, as shown in Fig. 2(d). Pure Si L (on set 99 eV) was recorded from the Si substrate to confirm the chemical shift (99–105 eV) of the interfacial layer.

3.3. Surficial length enhancement and dark current–voltage profiles

Under dark condition, current–voltage profiles were obtained for all three devices; this information is charted in Table 1. A turn-on current of 1 μA was reached at 0.612 V from a planar AZO/Si device. An equivalent current level was reached at a reduced voltage of 0.48 V from a 5/10 pillar-device. A further reduction of turn-on voltage was achieved from a 5/7 pillar-device. These results strongly suggest that the current values are directly affected by the device structures, even when using the identical materials.

At a fixed length, we can compare the surficial length of the pillar structures to that of a planar substrate (Fig. 3(b)). For a planar substrate, the surficial length is referred as 100%. According to the pillar structures, substantially enhanced surficial lengths were achieved: by 157% for the 5/7 pillar-arrays and by 147.6% for the 5/10 pillar-arrays.

Rectifying characteristics were investigated for the flat-Si, 5/10 pillar, and 5/7 pillar devices. The rectification ratios were obtained using values of the current at +1 V over the current at −1 V. A flat-Si device provided a relatively low rectifying ratio of 10.2. Pillar structured devices effectively improved the rectifying ratios. The 5/10 pillar device gave a rectifying ratio of 26; the 5/7 pillar device reached a value of 48.2. This implies that the enhanced performances can be attributed to the enlarged surficial length of the pillar structures. The enhancement of the surficial length is directly related to the interface region of AZO/Si, which proportionally extends the active area of a heterojunction.

The ideality factor (n) was obtained from the following equation to investigate the junction qualities of the three devices using the following equation:

$$n = \frac{q}{kT}\frac{\partial V}{\partial(\ln I)} = \frac{q}{kT}\frac{\partial V}{2.3 \times \partial \log I} \quad (1)$$

where q, kT, and I are the electron charge, thermal energy (eV), and current, respectively. For a flat-Si device, an n-value of 1.54 was obtained, which is a similar value to the previous report [11].

Table 1
Profiles for various AZO/Si heterojunction devices.

	Flat Si device	5/10 pillar device	5/7 pillar device
Surficial enhancement (%)	100	147.6	157
Current at +1 V (mA)	0.282	0.298	0.681
Current at −1 V (mA)	2.87	7.75	32.84
Rectifying ratio	10.2	26	48.2
Ideality factor	1.54	1.48	1.32

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