



## Facile integration of ordered nanowires in functional devices



Jordi Guilera<sup>a</sup>, Cristian Fàbrega<sup>a,b</sup>, Olga Casals<sup>b</sup>, Francisco Hernández-Ramírez<sup>a,b</sup>, Shuangzhou Wang<sup>c</sup>, Sanjay Mathur<sup>c</sup>, Florian Udrea<sup>d,e</sup>, Andrea De Luca<sup>d</sup>, S. Zeeshan Ali<sup>e</sup>, Albert Romano-Rodríguez<sup>b</sup>, J. Daniel Prades<sup>b,\*</sup>, Joan R. Morante<sup>a,b</sup>

<sup>a</sup> IREC, Catalonia Institute for Energy Research, San Adrià de Besòs, Spain

<sup>b</sup> Departament d'Electrònica and Institute of Nanoscience and Nanotechnology (IN<sup>2</sup>UB), Universitat de Barcelona, Barcelona, Spain

<sup>c</sup> Institute of Inorganic Chemistry, University of Cologne, Cologne, Germany

<sup>d</sup> Engineering Department University of Cambridge, Cambridge, United Kingdom

<sup>e</sup> Cambridge CMOS Sensors Ltd, Cambridge, United Kingdom

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### ABSTRACT

The integration of one-dimensional (1D) nanostructures of non-industry-standard semiconductors in functional devices following bottom-up approaches is still an open challenge that hampers the exploitation of all their potential. Here, we present a simple approach to integrate metal oxide nanowires in electronic devices based on controlled dielectrophoretic positioning together with proof of concept devices that corroborate their functionality. The method is flexible enough to manipulate nanowires of different sizes and compositions exclusively using macroscopic solution-based techniques in conventional electrode designs. Our results show that fully functional devices, which display all the advantages of single-nanowire gas sensors, photodetectors, and even field-effect transistors, are thus obtained right after a direct assembly step without subsequent metallization processing. This paves the way to low cost, high throughput manufacturing of general-purpose electronic devices based on non-conventional and high quality 1D nanostructures driving up many options for high performance and new low energy consumption devices.

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### 1. Introduction

One-dimensional (1D) nanostructures offer a convenient path for the synthesis of high-quality, almost defect free, crystals of non-industry-standard semiconductor materials, such as metal oxides (MOX) [1,2]. However, the integration of these materials in functional devices, with the necessary degree of order and complexity, is an open challenge that still hampers the exploitation of their potential in full [2,3]. Current bottom-up approaches rely on a complex combination of positioning methods (e.g. nanomanipulation, self-assembly, di/electrophoresis, etc.) [3–5], and connecting methods (e.g. UV, electron/ion beam, soft lithographies) [6–8]. This strategy is however far from reconciling technical requisites with cost requirements of the industry.

A decade of research efforts shows that the most advantageous nanodevice configuration requires either a single (or a few) nanowires running parallel between two electrodes [9] to thus

build up a well-defined conduction channel to be easily modulated by external stimuli (e.g. chemical or biological agents [10,11], light or radiation [12], external electric fields [13,14], etc.). This means explicitly avoiding random wire-to-wire conduction paths which inevitably appear in devices based on randomly oriented mats of 1D nanostructures [15].

In the particular case of metal oxide nanowire-devices, this configuration has successfully led to a high number of applications and proof-of-concept prototypes, proving their interest in high temperature and power electronics, in which highly miniaturized field-effect transistors of wide-band gap semiconductor are sought after [16–18].

On the one hand, and regarding gas detection applications, nanowire-based metal oxide sensors [19,20] display important advantages only accessible in ordered configurations [15]. Firstly, the large surface-to-volume ratio of nano-sized materials provides a systematic way to increase the influence of surface phenomena, such as the response to gases [21]. Secondly, nanowires are typically enclosed by well-terminated surfaces in well-defined crystal orientations, offering a reduced set of interaction sites with gases that render better reaction control, and in general good signal stability

\* Corresponding authors. Tel.: +34 934039159.

E-mail address: [dprades@el.ub.edu](mailto:dprades@el.ub.edu) (J.D. Prades).

[15]. Thirdly, the response dynamics of one or a few nanowires is theoretically faster, if compared to porous layers made of nanoparticles, since all the sensing material is simultaneously exposed to the changes in the gaseous environment [15]. Last but not least, the self-heating effect [22] of nanowire devices can be used to dramatically reduce the power consumption typical of standard MOX sensors (from mW in microdevices to  $\mu$ W in self-heated nanowires [23]) with faster heating/cooling times (in the ranges of ms [24]), in temperature modulated applications.

On the other hand and as far as photodetection applications go, metal oxide nanowires show high intrinsic photoconductive gain values [12,25] mainly linked to the high crystallinity and ultimately caused by the electron–hole separation processes at the surface [26]). Additionally, in contrast with structures based on randomly oriented materials, parallel nanowire arrangements enable uniform light absorption through all the photoconductor material. All in all, MOX nanodevices offer a big potential to build up highly sensitive photodetectors [27].

Anyhow, all these applications are mostly limited by the lack of simple, cost effective and scalable methods to transfer, precisely position and interconnect nanowires. Among the most promising approaches, macroscopically driven dielectrophoresis [5] seems to address the manipulation concerns in a cost effective manner; but so far, only for selected materials [5,28], and in highly specialized electrode configurations [4,18] and usually followed by a contact fabrication step.

Here, we present a facile and high throughput methodology to build up ordered arrangements of metal oxide nanowires, between a pair of conventional electrodes without the need of any subsequent micromanipulation, lithography or post-processing technique. Our results prove that the method, based on dielectrophoresis, is flexible enough to integrate different types of metal oxide nanowires (such as  $\text{SnO}_2$ , ZnO,  $\text{TiO}_2$ , etc.) and attain the functionalities and the advantages expected from individual nanowires.

## 2. Methods

### 2.1. Materials

To demonstrate the flexibility of our method, three different metal oxide nanowires were used as a proof of concept.

First, crystalline  $\text{SnO}_2$  nanowires were produced by chemical vapor deposition (CVD) of a molecular precursor  $[\text{Sn}(\text{O}^t\text{Bu})_4]$ , catalyzed with Au on top of a Si wafer and following a procedure reported elsewhere [29–31]. The products were longer than  $15 \mu\text{m}$  with typical diameters of  $30 \pm 10 \text{ nm}$ .

Second, ZnO nanowires were obtained by a hydrothermal process reported earlier [32]. In brief, an 80 nm thick seed layer of ZnO was sputtered on indium-doped tin oxide (ITO) glass. The ITO glass was then placed in the growth solution consisting of 0.02 M zinc nitrate, 0.015 M hexamethylenetetramine (HMTA), 0.004 M polyethyleneimine (end-capped, molecular weight 800 g/mol) and 0.024 M ammonium hydroxide. The solution was heated to  $88^\circ\text{C}$ , and after 3 h, ZnO nanowires of about  $6 \mu\text{m}$  in length with diameters from 120 to 180 nm were obtained. The resulting ZnO arrays were finally rinsed with Milli-Q water and dried in nitrogen flow. Third,  $\text{TiO}_2$  nanowires were obtained by ALD conformal coating of silicon nanowires growth (typical diameter of 100 nm and  $5\text{--}7 \mu\text{m}$  in length) by CVD with a conventional method [33]. Tetrakis(dimethylamino)titanium(IV) (TDMAT) was used as a titanium source during the ALD process and water as an oxidizing agent. Growth temperature was fixed at  $250^\circ\text{C}$  with a sequence of 5 s of TDMAT followed by 5 s of water. A total of 2500 cycles were applied to obtain 100 nm of  $\text{TiO}_2$ , corresponding to a growth rate of  $0.4 \text{ \AA}/\text{cycle}$ .

As for the substrates, commercial microhotplates ( $\mu$ HP) with Au Inter Digital Electrodes (IDE) from Cambridge CMOS Sensors ([www.ccmoss.com](http://www.ccmoss.com)) were used. These devices were originally designed to accommodate a gas sensitive layer across two IDE electrodes. No modification of the general-purpose IDE design was made to facilitate the here-proposed integration method. Gold is inert to oxidation and the rough Au surface provides better attachment to the later deposited nanowire, according to preliminary tests. The IDEs spanned a circular area of  $250 \mu\text{m}$  in diameter and the gap between the IDE fingers was  $10 \mu\text{m}$ . In order to reach the optimum operating temperatures, the devices also integrate a microheating element made of tungsten, and buried under the IDEs within  $\text{SiO}_2$  insulation, following an architecture reported elsewhere [34]. Unlike polysilicon heaters, the tungsten heaters offer a much higher stability at high temperatures. The circular  $\text{SiO}_2$  insulating membrane obtained by Deep Reactive Ion Etching (DRIE) embedding the IDEs/heater had a diameter of about  $640 \mu\text{m}$ . IDEs, and associated bond pads, were manufactured post-CMOS sequence. The maximum temperature the  $\mu$ HP can reach is about  $700^\circ\text{C}$ , while the power consumption is only about 55 mW at  $450^\circ\text{C}$ . In this work, the heating element was solely used for test and calibration purposes.

### 2.2. Integration methodology

The as-grown nanowires were first removed from their original substrates by means of sonication. To that end, the substrates were fully immersed in isopropanol and then submitted to an ultrasonic bath for a few minutes. Power and duration of the bath were adjusted to obtain dispersions with suitable nanowire concentrations in all cases.

For the nanowire integration in the  $\mu$ HPs and subsequent alignment between the IDEs, dielectrophoretic forces were used [5] applying an AC square signal (15 V peak-to-peak) to the electrodes. One or more drops of the nanowire's dispersion were deposited on top of the IDE using a microsyringe. The frequency of the signal was then adjusted for each material to achieve an optimum coverage and alignment of nanowires.

After the deposition and induced alignment of the nanowires across the IDE, the resulting devices were kept at  $100^\circ\text{C}$  for 2 h to facilitate the full evaporation of the solvent residues.

### 2.3. Device test and characterization methods

The resulting devices were first electrically tested; current–voltage ( $I$ – $V$ ) curves were acquired with a dual-channel Keithley SourceMeter Unit (SMU) model 2600 and custom-made LabView software. Shielded coaxial wires, fixings and test chambers were used to minimize noise in the electrical measurements due to the high resistance of some devices. In temperature controlled experiments, the microheater of the  $\mu$ HPs was also powered by the second SMU channel of the same instrument. The calibration curves provided by the manufacturer and in-house validated were used to estimate the temperature reached by the  $\mu$ HP. The direct comparison of the device resistance values at different microheater operating conditions and those obtained as a function of increasing current level without the heater was used to estimate the equivalent temperature reached due to the self-heating effect [23,35].

In gas sensing experiments, accurate gaseous environments were maintained inside the test chamber with mass flow controllers mixing dry synthetic air (SA, 21%  $\text{O}_2$  and 79%  $\text{N}_2$ ), and CO ( $100 \text{ ppm} \pm 1\%$  in SA). These lab-class gases contained less than 5 ppm/vol of  $\text{C}_n\text{H}_m$  and  $\text{H}_2\text{O}$ .

For experiments under illumination, a Hammamatsu LC8 light source with a type [–01] Hg–Xe lamp enhanced for the line at  $\lambda = 365 \text{ nm}$  was used. UV light intensity impinging on the devices

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