Sensors and Actuators B 185 (2013) 713–719

Contents lists available at SciVerse ScienceDirect

Sensors and Actuators B: Chemical

journal homepage: www.elsevier.com/locate/snb

Metal-coated silicon micropillars for freestanding 3D-electrode arrays in microchannels

Samuel C. Kilchenmann[a,*,1], Enrica Rollo[a,1], Elena Bianchi[a,b], Carlotta Guiducci[a]

[a] Laboratory of Life Sciences Electronics, Ecole Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland
[b] Laboratory of Biological Structure Mechanics, Department of Chemistry, Materials and Chemical Engineering 'Giulio Natta', Politecnico di Milano, 20133 Milano, Italy

ARTICLE INFO

Article history:
Received 25 February 2013
Received in revised form 3 May 2013
Accepted 8 May 2013
Available online 24 May 2013

Keywords:
Silicon microfabrication
3D electrodes
Microelectrode arrays
Lab-on-a-chip
Cell manipulation and analysis

ABSTRACT

This paper presents a fabrication process for arrays of high-aspect-ratio micropillar electrodes, which are freestanding 3D structures that feature metal sidewalls connected to passivated planar wires. Facing vertical electrodes are considered to be a key solution in microdevice technologies, as they are able to improve the efficiency and accuracy of electrical methods by generating homogeneous electric fields along the height of microfluidic channels. Despite the acknowledged advantages of using vertical microelectrodes, current microfabrication technologies do not allow the manufacture of such structures with the same resolution and versatility as planar electrodes. The present study focused on the fabrication of round and square-shaped silicon pillar arrays exposing metal on their sidewalls, which is decoupled from the substrate by means of a passivation layer. The pillars range in width from 10 μm to 70 μm, with gaps down to 10 μm and a maximum aspect ratio of 5:1. Metal deposition and patterning were revealed to be the critical steps of the process. Deposition was achieved by sputtering, while patterning was performed by photolithography, and the photoresist was applied by spray-coating. The pattern was then transferred into the metal layer by means of dry etching. This new process can be adapted to any metal that is suitable for depositing by sputtering and patterning by dry etching. The presence of the metal layer on the vertical sidewalls was confirmed by SEM imaging combined with EDX analysis. The arrays were then characterized by electrical conductivity measurements and impedance spectroscopy.

1. Introduction

Electrical signals have been used for a wide range of applications in microfluidic or lab-on-a-chip devices. Cell and particle counting has been achieved with on-chip coulter counters [1–3], while impedance spectroscopy has been applied to study particles and to extract their electrical parameters [4], and dielectrophoresis has been used to sort and move specific cells and particles depending on their electrical characteristics [5]. Furthermore, electrical fields are used to manipulate cells. The high resolution of microfabrication technologies makes it possible to apply high and localized electric fields that can be used for the electroporation of cells [6,7]. The same principle can be used to lyse complete cells, as several research groups have shown [8–10]. It has also been shown that cell fusion can be induced through the application of an electric field between two cells [11].

The characteristics of the electrodes play an important role in all of these techniques. The simplest electrode configuration consists of planar electrodes that are deposited on the bottom of microfluidic channels. While the fabrication of such electrodes is easy, this configuration results in heterogeneous fields in the channel. For higher channels in particular, it is hard to reach fields that are strong enough over the whole channel height to be suitable to sense or manipulate particles. Better results can be achieved by placing the electrodes so that they face each other. Such an arrangement means that the induced fields exhibit better linearity in between the electrodes, which makes it possible to achieve improved field homogeneity throughout the channel [12,13]. Two main configurations lead to facing electrodes. The electrodes can either be placed at the top and bottom of a chamber, or they can be fabricated parallel to the channel's sidewalls. In the first case, the top and bottom electrodes must be fabricated separately on two substrates that must then be aligned and bonded together. Also, packaging for such devices is critical, since the electrical contacts of the chips face one another, making it impossible to simply use wire-bonding.

In the second case, the electrodes are placed parallel to the sidewalls and are fabricated and connected on the same substrate. Such electrodes have been fabricated by such methods as etching microfluidic channels into highly doped silicon [14]. Another approach involves obtaining so-called "vertical liquid electrodes" on the channel sidewalls by electric current injections in the

* Corresponding author. Tel.: +41 216931106.
E-mail address: samuel.kilchenmann@epfl.ch (S.C. Kilchenmann).
[1] These authors contributed equally to this work.

0925-4005/$ – see front matter © 2013 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.snb.2013.05.037

channel by planar electrodes in dead-end chambers placed perpendicular to the main flow [15]. Sidewall electrodes can also be obtained by combining wet etching and metal deposition in order to develop elliptic-like channels with electrodes on their internal surfaces [16]. Furthermore, electrodes were fabricated from polymers such as PDMS that turned conductive by mixing them with metal ions [17] such as gold or silver [18], with carbon black particles [19] or with single and multiwall carbon nanotubes [20].

In the two outlined solutions for realizing facing electrodes, the electrode distance is determined either by the channel width or height. The advantage of freestanding electrodes, on the other hand, is that electrode gaps can be designed with more flexibility. This additional degree of freedom makes it possible to design smaller gaps, leading to higher field strength. Furthermore, freestanding 3D electrodes make it possible to increase the sensing volume of a sensor, while keeping the distance between the electrodes and the passing particles small. Accordingly, higher throughput can be achieved without affecting efficiency or performance. Moreover, applied potentials can be reduced while achieving the same field strengths.

Freestanding pillar electrodes in microfluidic channels will obviously introduce additional flow resistance and lead to flow disturbances that might be critical for some applications. Nevertheless, freestanding pillar electrodes might also be integrated into channel sidewalls [13], if needed, in order to avoid flow disturbances caused by the pillars.

Although freestanding pillar electrodes offer advantages for electrical-based techniques, their implementation entails specific fabrication challenges. Different processes for such structures have been proposed. Electroplating has been used to realize pillar electrodes consisting of metals [21] or conductive polymers [22]. 3D carbon structures have been realized by patterning thick photoresist that was subsequently turned into conductive carbon structures (CMEMS) by means of pyrolysis [23]. Freestanding carbon structures have also been fabricated by replica moulding of carbon black particles into microfluidic devices [24]. 3D MEAs have been fabricated by a method that combines sputtering, laser-scribing and electroplating [25].

All of the above-mentioned technologies have some drawbacks. In the case of electroplating, process parameters must be accurately controlled in order to achieve good surface properties of the structures. Moreover, the geometry of the structures also has an influence on their surface properties, resulting in design constraints. In cases where electroplating is used in conjunction with laser-scribing, the same problems and restrictions arise over the additional fabrication complexity, making it a long and expensive technology. CMEMS are a cost-effective alternative to the above-mentioned technologies, but the resulting carbon structures have a conductivity that is some orders of magnitude lower than similar metal structures. Furthermore, the shrinkage of the precursor during the pyrolysis step must be taken into consideration during the design phase and also limits the types of shapes that can be obtained. Moreover, the shrinkage observed during pyrolysis almost does not affect the bottom of the pillars where they adhere on the substrate. For this reason, the pillars have the original diameter close to the substrate and then shrink with height, making it difficult, especially for smaller pillars, to achieve uniform gap widths over the full channel height.

With replica moulding of carbon black particles, on the other hand, the resolution and design restrictions correspond to the ones related to the fabrication of the micromould masters. The main drawback of this technology is the high resistivity of the electrodes, which are made from a mixture of PDMS and carbon black particles.

The present paper proposes a new fabrication process that is based on the combination of sputtering and evaporation to selectively deposit conductive and insulating layers, either on the entire wafer surface or only on horizontal planes. In this way, silicon pillars are first passivated and then covered with platinum. Horizontal metal layers are patterned by spray coating and dry etching, and the resulting horizontal features are passivated through the evaporation of a silicon dioxide layer. The choice of materials was motivated by the widespread use of these materials for life science applications; however, any conductive material that can be deposited by sputtering can be used for the electrodes and any insulating material that can be evaporated can be used for insulation purposes. The fabrication process was optimized for arrays of 50 μm high round and rectangular-shaped pillars with sizes ranging from 10 to 70 μm. Arrays with inter-pillar spacing down to 10 μm were achieved. The main advantages of this fabrication process are good control of geometrical features of the pillars, excellent surface quality of the electrodes and a wide range of possible materials that can be employed.

2. Materials and methods

2.1. Microfabrication process

The micropillars were obtained on 4″ silicon wafers. For this purpose, first a 4 μm positive tone photoresist (thinned AZ 9260) layer was applied by spin coating. The resist was exposed on a mask aligner (Karl Süss MA/BA 6) with a dose of 220 mJ/cm^2. After the resist was developed, the pattern was transferred into the silicon using a Bosch process (Alcatel AMS 200 DSE) targeting a final etch depth of 50 μm. The entire wafer was passivated by chemical vapor deposition (Centrotherm furnace) of either silicon nitride (Si_3N_4 500 nm) or silicon dioxide (SiO_2 1 μm). A platinum layer with a titanium adhesion layer (Ti/Pt 20/200 nm or 20/140 nm) was then sputtered (Pfeiffer SPIDER 600) on the wafer.

For adhesion purposes of a final passivation layer, an additional layer of titanium (20 nm) was evaporated on top of the platinum (Leybold Optics LAB600H). Evaporation was chosen for this specific layer formation in order to avoid depositing titanium on the vertical sidewalls of the pillars where only platinum is meant to be exposed to the solution.

For the patterning of the metal layers, a diluted AZ photoresist (AZ 9260:PGMEA:MEK 4:8:90) was spray-coated in three superposed layers with successive baking steps for each layer (EVG 150). A short treatment with oxygen plasma (30 s 500 W, 400 ml/min, Tepla 300) was performed prior to spray coating. The resist was exposed with a dose of about 780 mJ/cm^2 on a standard mask aligner (Karl Süss MA/BA 6) and developed by an automated development system (EVG 150). The pattern was then transferred into the metal layer by dry etching (STS Multiplex ICP). After photoresist removal, an additional cleaning with piranha solution was performed to remove resist residues.

Finally, for the purposes of electrical insulation, a 200 nm thick SiO_2 layer was evaporated on the horizontal surfaces (Leybold Optics LAB 600H).

2.2. Electron microscopy characterization of micropillar arrays

Two different Scanning Electron Microscopes (SEM, ZEISS LEO and ZEISS MERLIN) were used to observe the patterning of the metal layer inside the gaps. For this purpose, we realized arrays of 50 μm high pillars with different shapes (square and round), dimensions (10–70 μm) and gaps (10–60 μm).

An energy dispersive X-ray detector (EDX, Oxford Instruments EDX X-MAX) mounted on the ZEISS MERLIN was employed to analyze the material composition of the vertical sidewalls. Data were treated by the AZTEC software (Oxford Instruments).