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Gate-induced drain leakage current characteristics of p-type polycrystalline silicon thin film transistors aged by off-state stress

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ABSTRACT

Thin film transistors have become crucial components of several electronic display devices. However, high leakage current is a frustrating impediment to increasing the efficiency of these transistors. We have performed an experimental and quantitative study on the effects of off-state bias stress on the characteristics of a p-type polycrystalline silicon (poly-Si) thin film transistor (TFT). The gate-induced drain leakage (GIDL) current under off-state bias stress conditions was investigated by changing gate-source voltage (V_{gs}) and drain-source voltage (V_{ds}). Off-state bias stress was found to dramatically increase the threshold V_{gs} from 1 to 11 V, thereby increasing the voltage needed to turn off the TFT, without causing significant changes in on-state current or subthreshold swing. We developed local defect creation and charge trapping models for a technology computer-aided design simulation platform to understand the mechanisms underlying these observed effects. Using the model, we showed that off-state stress induces charge trapping within the local defects of a high electric field region in the TFT channel near the drain. This reduces the electric field and thermionic field-emission current, which in turn lowers the GIDL current by increasing threshold voltage V_{gs}.

1. Introduction

Polycrystalline (poly) silicon (Si) thin film transistors (TFTs) are generally used in active matrix display devices because of their multiple advantages [1]. The high field effect mobility of poly-Si TFTs is important for peripheral circuits such as gate and emission drivers. Therefore, poly-Si TFTs can be easily integrated into display panels and are suitable for high resolution applications. Furthermore, the stability of poly-Si TFTs is very high under electrical and optical stress, making it a very popular device for use in active matrix organic light emitting diodes (AMOLEDs) and active matrix liquid crystal displays (AMLCDs) [2].

Despite these advantages, the poly-Si TFT is limited by high leakage current resulting from defect states in the poly-Si grain boundary. As the demand for display panels with ultra-high density resolution increases, there is an urgent need for efficient short-channel TFTs to form the individual pixels of AMOLED displays. This has prompted careful studies on the problem of leakage current in poly-Si TFTs [3]. Gate-induced drain leakage (GIDL) resulting from high drain-source voltage (V_{ds} > 5 V) has been of particular concern, because the switching TFT of the AMOLED is normally operated under high gate bias conditions [4].

Several attempts to reduce the leakage current in poly-Si TFTs have been described in the literature [5]. Lightly doped drain (LDD) and offset structures can reduce the leakage current by reducing the electric field near the drain edge in the poly-Si channel, but instead, these methods reduce the field effect mobility to result in less drain current at on-state. Thermal and plasma treatments have also been reported to reduce the leakage current resulting from defects in grain boundaries of poly-Si [6], which need additional processing requiring more time and costs. For these reasons, they have not been widely applied in the fabrication of display devices.

Another approach that has been proposed to reduce leakage current in p-type poly-Si TFTs is based on off-state stress [7,8]. Off-state stress in a fabricated p-type poly-Si TFT is to apply positive gate-source voltage (V_{gs}) and negative drain-source voltage V_{ds} of 5 to 15 V and −3 to −40 V respectively to the TFT for a short time. In our study, following the generation of off-state stress, the minimum leakage current was not found to have changed, but the threshold V_{gs} (the V_{gs} required to induce current, including GIDL) was considerably elevated. The GIDL current was correspondingly reduced and did not increase after the TFT was subjected to annealing at 250 °C. Importantly, field effect mobility and

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subthreshold characteristics were not degraded.

Previous studies have demonstrated GIDL reduction and addressed several possible reasons for the GIDL current reduction [7,8]. However, for the off-stress of the poly-Si TFTs, the physical phenomenon was not yet numerically explained, and the characteristics of the GIDL current induced in poly-Si TFTs have so far not been properly reported. In this work, we conducted a technology computer-aided design (TCAD) simulation and analyzed characteristics of a pristine poly-Si TFT and those of the same TFT aged by off-state stress to find the key factor of the GIDL current reduction. The aged GIDL current generated by off-state stress was described in the TCAD simulation to understand the underlying cause of the observed differences. We investigated possible causes of suppressing GIDL current based on the M.J. Powell's work especially related with the charge trapping and defect creation [9]. Especially, we experimentally and numerically investigated the role of gate-drain voltage (V_{gd}) in suppressing the GIDL current, which is related with charge trapping in the gate oxide, by using TCAD simulation. Moreover, we compared on- and off-characteristics of experimental and numerical results, and we also experimentally and numerically studied the activation energy of the GIDL current after the off-stress. This work can provide numerical explanations for the physical mechanism of the GIDL current reduction by off-state stress-based aging, which will be useful for the development of reliable poly-Si TFT devices.

2. Experimental methods

2.1. Fabrication of the poly-Si thin-film transistor

A 300-nm-thick buffer oxide layer and a 50-nm-thick amorphous silicon (a-Si) film were deposited sequentially on a glass substrate. The a-Si film was dehydrogenated at 400 °C under nitrogen gas (N_2)-based ambient conditions for 10 min and crystallized using a xenon chloride (XeCl) laser with a wavelength of 308 nm. The energy density of the laser was optimized to be between 300 and 500 mJ/cm^2, and the grain size of the crystallized poly-Si film was approximately 300 nm. A 130-nm-thick silicon dioxide (SiO_2) film was deposited as a gate insulator, and then a molybdenum gate metal layer was deposited and patterned over the SiO_2 layer. The ion shower for source and drain doping of boron was performed. The source and drain were annealed at 400 °C under N_2-based ambient conditions for approximately 2 h. An interlayer SiO_2 was then deposited, followed by deposition of source and drain metals. In this work, we use a molybdenum/aluminum/molybdenum multi-layered metal structure, which is commonly used because of its good metal contact property. The channel width and length of the fabricated TFTs are 3 and 4 μm, respectively. The electrical properties of the TFT in its pristine condition were measured using a semiconductor parameter analyzer (Agilent 4156C) in dark-room conditions.

2.2. Aging of the TFT under conditions of off-state stress

In an attempt to suppress the GIDL current, the fabricated poly-Si TFT was aged by inducing off-state stress using the parameter analyzer. Generally, since the highest voltage is applied between the gate and drain, the applied stress voltage is algebraically defined as the gate-drain voltage V_{gd} ($= V_{gs} - V_{ds}$). The relationship between time and the effects of stress on electrical characteristics was not fully understood yet, but it has been reported that the electrical behaviors after the stress are similar regardless of the stress time from 1 to 1200 s [7]. Thus, we have varied the off-stress from 10 to 60 s, repeatedly, and have achieved similar results so that aging time was fixed at 10 s, which is a long enough time for a stable off-state stress effect.

First, drain current (I_d) characteristics at on- and off-states were investigated for off-state stress voltage V_{gd} varying between 15 and 35 V, by setting V_{gs} and V_{ds} between 10 and 20 V, and −5 and −15 V respectively. To further investigate the effect of stress, we then fixed the value of V_{gd} at 25 V, varying V_{gs} and V_{ds}. GIDL was measured under these conditions.

2.3. TCAD simulation to study TFT aging by off-state stress

A TCAD simulation was used to understand the aging phenomenon. First, the current and voltage behaviors of the pristine poly-Si TFT were emulated by fitting the density of states (DOS) function for poly-Si into the TCAD simulations. The on-state and subthreshold drain current characteristics were well-represented by the double exponentially-distributed DOS. To describe leakage characteristics, a band-to-band tunneling model (Hurkx model) was used [10].

Another important purpose of the TCAD simulation was to understand the underlying cause for the discrepancies observed between pristine and aged TFTs, but the simple poly-Si TFT model of TCAD could not fully describe the characteristics of poly-Si TFTs aged by off-state stress. Therefore, we modelled TFTs with altered channel dimensions and also designed simulations based on two theories: local defect creation and charge trapping. Not only drain current behavior but also the atomic-level properties within the aged TFT such as tunneling carriers and electric field in the channel were presented as the results of the TCAD simulation that together described the aging effect. Finally, in order to verify the TCAD simulation, we estimated activation energies of the GIDL current in pristine and aged TFTs.

3. Results and discussion

Fig. 1 represents results from the analysis of the fabricated poly-Si TFT aged by off-state stress. Fig. 1(a) shows the on-state and subthreshold drain current (I_d) characteristics are slightly increased. The charge carrier mobility of the poly-Si TFT which was 95 cm^2/V s initially, increased to 95, 96, 101, and 104 cm^2/V s when the V_{gd}

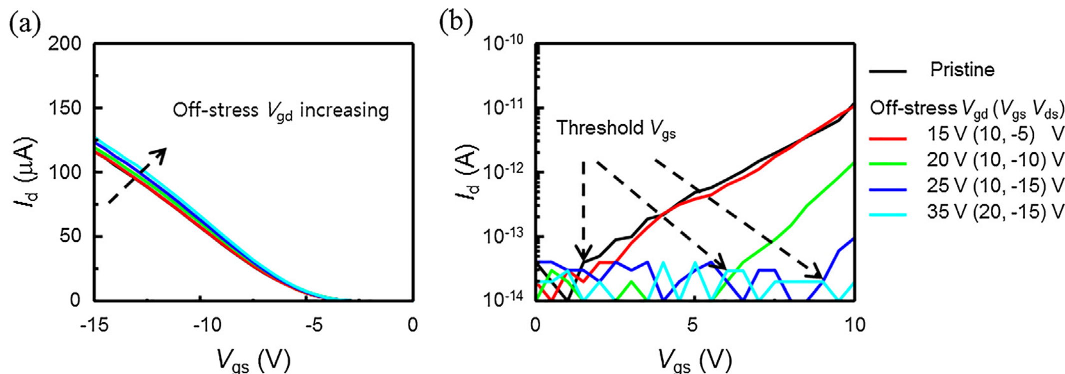

Fig. 1. Gate voltage versus drain current transfer characteristics of pristine and aged samples, measured at V_{ds} = −5.1 V for the various V_{gd} off-stress voltage. (a) On-state and subthreshold characteristics, and (b) off-state characteristics as functions of off-state stress (off-stress) inducing voltages (V_{gs} and V_{ds}).

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