A Novel Charge Recycle Read Write Assist Technique for Energy Efficient and Fast 20nm 8T-SRAM Array

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PII: S0038-1101(18)30159-X
DOI: https://doi.org/10.1016/j.sse.2018.07.005
Reference: SSE 7448

To appear in: *Solid-State Electronics*

Received Date: 16 March 2018
Revised Date: 2 July 2018
Accepted Date: 16 July 2018

Please cite this article as: Nayak, D., Priyabrata Acharya, D., Kumar Rout, P., Nanda, U., A Novel Charge Recycle Read Write Assist Technique for Energy Efficient and Fast 20nm 8T-SRAM Array, *Solid-State Electronics* (2018), doi: https://doi.org/10.1016/j.sse.2018.07.005

A Novel Charge Recycle Read Write Assist Technique for Energy Efficient and Fast 20nm 8T-SRAM Array

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Abstract

The read instability of conventional 6T-SRAM cell has made the 8T-SRAM cell a substitute for high data reliability. But the single ended nature of read operation demands a complete V_{dd} swing of high capacitive read bit lines leading to large energy consumption. A novel assist technique using charge recycling concept is proposed here which reduces the read and write energy by reducing the voltage swing. Mathematical analysis of the proposed technique, theoretically predicts the read and write energy to reduce by 75% and 25% respectively compare to that of the conventional 8T-SRAM array. Experimental simulation using predictive technology model demonstrates these two energy consumptions to be reduced by 58% and 27% respectively. The proposed technique also reduces the leakage current flow in the standby cells and hence the energy consumption. The dummy read current flow in the half-selected cells is also controlled significantly in the proposed technique. The stability of the SRAM cell remains unchanged by the insertion of the proposed assist technique.

Keywards- SRAM, Assist technique, Charge recycling, Half-selected cell, Leakage current

1. INTRODUCTION

SRAM is the main on chip memory technology having wide applicable domain. ITRS roadmap projects that on-chip memory is going to occupy major portion of modern system on chip (SoC). The energy consumption of SRAM constitutes a significant portion of total energy consumption of the chip. Though supply voltage scaling is widely used for power reduction in SRAM based memory, it degrades the data stability for the destructive nature of read operation. 8T-SRAM is a prominent candidate in low power applications eliminating the destructive read process of 6T-SRAM cell leading to higher data stability. However 8T-SRAM consumes significant amount of energy during data read to swing the high capacitive bit lines. Reduction of energy consumption in 8T-SRAM memory array is a major challenge in on-chip memory design. Besides this a fast performing memory is a highly desirable feature in modern system.

Several techniques have been proposed to reduce energy consumption of SRAM array by limiting the voltage swing of the bit lines. The write energy is reduced by recycling the bit line charge with the neighboring bit lines [1]. Charge sharing between more columns leads to a low voltage difference between bit line pair of a particular column restricts the write robustness. Generation of

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