Solid State Electronics 148 (2018) 51–57

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Investigation of avalanche ruggedness of 650 V Schottky-barrier rectifiers

A. Konstantinov[a,*], H. Pham[b], B. Lee[b], K.S. Park[b], B. Kang[b], F. Allerstam[a], T. Neyer[c]

[a] ON Semiconductor, Isafjordsgatan 22, 16440 Kista, Sweden
[b] ON Semiconductor, 420711 Bucheon, Republic of Korea
[c] ON Semiconductor, 85609 Munich, Germany

ARTICLE INFO

The review of this paper was arranged by Prof. A. Zaslavsky

Keywords:
Avalanche breakdown
Schottky diodes
Silicon carbide

ABSTRACT

Avalanche breakdown of novel 650 V SiC Schottky-barrier rectifiers is investigated. The rectifier diode has low leakage current for the temperatures up to 300 °C. Thermal coefficient of avalanche breakdown increases with the temperature to around 0.009%/K at 200 °C. Near-uniform avalanche breakdown is verified using emission imaging, and maximum specific avalanche energy of 20.7 J/cm^2 is achieved. The critical temperature for stability in unclamped inductive switching (UIS) is above 520 °C as estimated through thermal simulation. Long-term walkout of breakdown voltage at 176 °C is less than 0.02%.

1. Introduction

Silicon carbide Schottky-barrier diode (SBD) rectifiers are increasingly used in high performance power conversion systems in order to minimize system size and power loss. However, possible reliability and ruggedness issues with new materials like SiC are of concern for system designers [1]. Such concerns are aggravated by insufficient understanding of breakdown in high-voltage SiC devices. In this study we perform investigation of avalanche breakdown in novel 650 V Schottky-barrier rectifiers with improved avalanche ruggedness. We investigate temperature-dependent leakage currents, study the uniformity of avalanche breakdown using emission imaging, and perform a study of unclamped inductive switching (UIS) so as to determine the maximum sustained avalanche energy and to determine the critical temperature for thermal runaway.

2. Device fabrication and basic properties

The 650 V rectifiers studied in this work have a junction-blocked Schottky (JBS) design, which is a lower-voltage version of the 1200 V rectifier diode earlier reported in [2,3]. This JBS employs a linear array of closely spaced p-bodies to shield the Schottky metal from high electric field. The p-bodies are formed by multiple-energy acceptor doping implant into an n-type epitaxial layer grown on 6-inch low-resistivity n-type 4H SiC substrate, 4° off the basal plane towards [11$\bar{2}$0]. Linear p-bodies are oriented parallel to the substrate off-orientation direction. Ion implantation was employed to form the junction termination region in order to mitigate electric field concentration at the diode periphery. Ion implants were activated using high-temperature anneal, after which the topside metal stack was deposited and patterned. The topside metal was Ti/TiN/Al-Cu. An inorganic passivation dielectric was deposited and patterned at the device periphery; and a polyimide layer at the device periphery was also provided for additional protection. The diode wafers were thinned down to 200 µm. Nickel silicide Ohmic contact was formed at the substrate backside using pulsed laser anneal. Ti/Ni/Ag metal stack was deposited onto the nickel silicide so as to form solder metal. Wafers were diced, and chips were packaged into standard TO-type epoxy-mould packages. Some device properties were investigated on-wafer, such as emission images, as well as reverse blocking at very high temperatures, which temperatures might exceed the thermal limit of the epoxy mold compound (EMC) employed.

Our JBS design utilizes a trench structure, in which the p-bodies are implanted into etched trenches, so as to increase the depth of shielding p-bodies improving electrostatic shielding of the Schottky barrier metal. Graded profiles of the anode implant are employed so as to avoid the effects of excessive electric field crowding and of early breakdown at the edges of the shielding p-bodies. High voltage termination is provided using multiple-zone junction termination extension (JTE), in which the acceptor charge gradually decreases from the anode edge towards device periphery. Schematic cross-section of the rectifier is shown in Fig. 1.

Mean forward drop at rated current is around 1.42 V at room temperature (RT) and it increases to 1.7 V at 175 °C. The active-area current density is around 530 A/cm^2 at rated current. The rectifier diodes for a lower current rating had the active-region area scaled down in

* Corresponding author.
E-mail address: andrei.konstantinov@onsemi.com (A. Konstantinov).

https://doi.org/10.1016/j.sse.2018.07.011
Received 23 March 2018; Received in revised form 2 July 2018; Accepted 24 July 2018
Available online 25 July 2018
0038-1101/

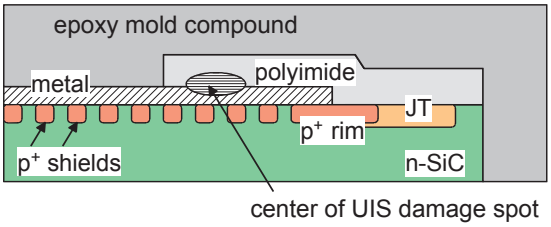

Fig. 1. Schematic cross-section of packaged 650 V Schottky-barrier rectifier. Schematic cross-section of packaged SBD chip and location of UIS failure. Hard-dielectric passivation over the junction termination (JT) region and anode trenches are omitted in the drawing.

proportion to the rating. Typical leakage current at 650 V is 7 μA at 175 °C for the 30 A device. Avalanche breakdown voltage is typically between 750 V and 800 V.

3. Leakage currents and temperature dependence of breakdown

Leakage currents at high temperatures were investigated on-wafer. We did not observe discharge flashover for on-wafer studies of breakdown at the voltages of around 700–800 V, unlike the case for 1200-V rated devices. Breakdown could therefore be investigated without using any dielectric liquids or of a high-pressure enclosure. Shown in Fig. 2a are reverse-bias characteristics for the temperature range between 25 °C and 300 °C. This device had a current rating of 6 A. It is seen from the plots that reasonably low reverse current can be achieved with the Ti Schottky barrier up to around 300 °C. Low leakage current at 300 °C is hardly required for normal device operation because of the package limitations, however a lower leakage also means potentially higher critical temperature for thermal runaway in avalanche. The latter is an advantage from the viewpoint of device ruggedness.

It is seen from Fig. 2a that the breakdown voltage is increasing with increasing temperature, as it is generally expected for avalanche breakdown due to reduction of the ionization rates at elevated temperatures. For comparison of reverse currents between JBS and p-n diodes we refer to Fig. 2b. Plotted in Fig. 2b are the room-temperature leakage currents for 6 A 650 V JBS and for a test p-n diode on the same wafer, which p-n diode has the same size and the same junction termination as the JBS. Much lower leakage currents are observed for the p-n diode because minority carrier generation in a p-n diode requires an electron overcome a higher barrier than that in a Schottky diode. However the I-V characteristics of p-n and JBS diodes become nearly identical near the point of breakdown. We conclude that the avalanche breakdown in our JBS rectifiers is very close to that in a parallel-plane p-n diode.

Temperature dependence of the breakdown voltage was extracted from another set of on-wafer measurements, which were done in pulsed mode in the temperature range of 25 °C–325 °C. Pulsed current-voltage characteristics were approximated by a linear dependence for a peak current in the range of between 10 mA and 20 mA. Avalanche breakdown point was assigned to a current of 15 mA. This routine closely follows the technique earlier applied by Rupp et al. in [4]. Resulting temperature dependence of the breakdown voltage is plotted in Fig. 3a; and the temperature coefficient of breakdown voltage (*TK*) is plotted in Fig. 3b.

The temperature dependence observed in this study is substantially weaker than that observed by Rupp et al. [4], who earlier investigated silicon carbide JBS rectifiers having a breakdown voltage very close to that of ours. Rupp et al. reported almost constant temperature coefficient of 0.018%/°C for the temperature range between 25 °C and 175 °C. Several reasons could be responsible for the difference in temperature dependence. One possibility is related to anisotropy of avalanche breakdown in SiC. For a near-isotropic material like silicon or GaAs the temperature coefficient of breakdown voltage is almost independent on device configuration for a fixed value of the breakdown voltage. However, hexagonal SiC is an anisotropic material. Rupp et al. designed their Schottky rectifiers so as to achieve significant electric field concentration at the edge of each shielding p-body in order to lower the breakdown voltage in the active region and to minimize hot-carrier stress on the termination region. By contrast, our JBS rectifiers have the breakdown voltage very close that of parallel-plane breakdown, as we discussed it earlier in relation to Fig. 2b. This difference in design might affect the temperature dependence of breakdown. Unlike the case for silicon, hexagonal SiC has strong anisotropy for the critical field along different crystal directions, as well as for its temperature dependence [5]. According to [5], a higher extent of lateral electric field is expected to enhance the temperature dependence of breakdown voltage as compared to that for electric field parallel to the hexagonal axis. The difference in design between the diodes reported by Rupp et al. and those of the present study indeed correlates with the difference in temperature dependence.

Another possible cause of difference in temperature dependences are a contribution of deep-level traps to the temperature dependence of breakdown voltage. Such traps will have strongly non-equilibrium electron or hole occupancy factor at low temperatures if the free carriers due to breakdown are present in the space charge region. However, at high temperatures the trap occupancy factor will be

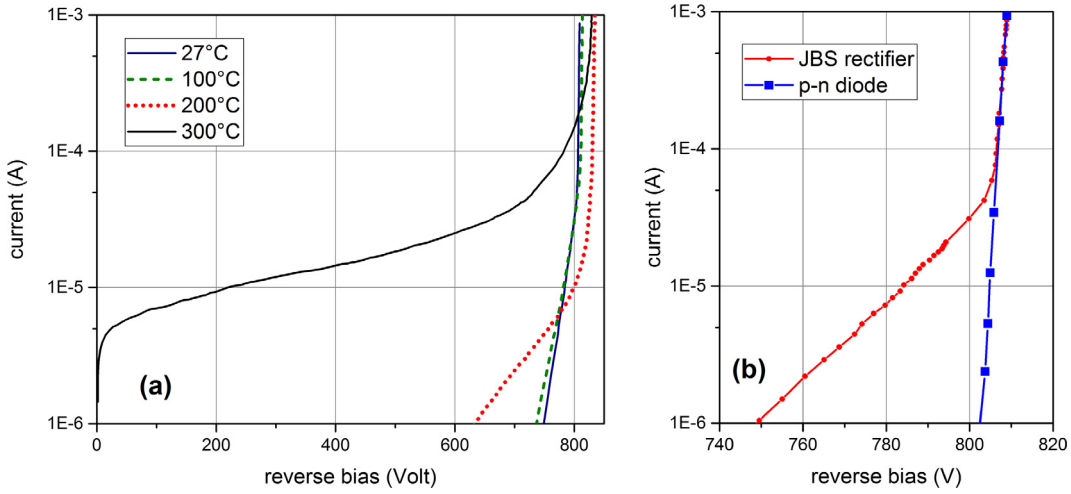

Fig. 2. Temperature-dependent reverse current of 6-A 650 V Schottky rectifier (a) and comparison of room-temperature reverse current of a Schottky rectifier with a test p-n diode of the same size formed on the same wafer (b).